Digital Voltmeter Series SM214

Instruction Manual

SM214

485

MP MASTER
MA24013

GEC Turbine Generators Ltd.
Grain Power Station
Isle of Grain
Rochester
Kent.

Instruction Manual

DIGITAL VOLTMETER

Series

SM 214

Issue 2

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AMENDMENT LIST NO.1.
TO
DIGITAL VOLTMETER SM 214 MANUAL

1. HAND AMENDMENTS

Section	Table	Figure	Change
6	6.3	-	Transistor TR 20 changed to Siliconix, E 112, S.E.L. Part No. BS 3157.
6	6.8	-	Capacitor C2 changed to 10µF tantalum, type TAG 10/16, S.E.L. Part No.CS 30991.
6	6.10	-	Capacitor C26 changed to 220 pF, ±10%, 160 V, Suflex, S.E.L. Part No. CS 30252.
7	-	1	Transistor TR 20 changed to E 112.

LIST OF AMENDMENTS

Al.No.	By Whom	Date	Al.No.	By Whom.	Date.

PREFACE

DAMAGE IN TRANSIT

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SECTION 1

SPECIFICATIONS

1, DIGITAL VOLTMETER SM 214

Full scale:	109999
Maximum Resolution:	10 μV on 1.1 V range.
Ranges:	4 d.c. voltage ranges as follows: 1.1V, 11V } direct 110V, 1.1kV } attenuated **Note:** 110mV d.c. range and a.c. ranges are not operational on basic SM 214.
Input Impedance:	Direct ranges: >5000MΩ Attenuated ranges: 10MΩ ± 0.1%
Input Current:	<50 pA, typically <20 pA.
Accuracy:	
24 Hrs. (+24°C ± 1°C):	All ranges: ± 0.002% of input, ± 0.002% of range
90 days (+20°C to +30°C):	(i) Direct Ranges: ± 0.005% of input, ± 0.002% of range (ii)Attenuated Ranges: ± 0.007% of input, ± 0.002% of range
1 year (+20°C to + 30°C):	(i) Direct Ranges: ± 0. 008% of input, ±0.002% of range (ii)Attenuated Ranges: ±0.01% of input, ±0.002% of range
Temperature Coefficients of Reading — outside normal operating range (0°C to +20°C and +30°C to +50°C):	(i) Direct Ranges: 0.0005% of input per °C. (ii)Attenuated Ranges: 0.0006% of input per °C. (iii)Zero: 0.0001% of range per °C.
Zero Stability:	Better than 0.002% of range for 90 days, 1 hour after switch-on.
Warm-up Time:	20 minutes to reach 1 year accuracy. 1 hour to reach 90 days accuracy.

Noise Rejection

Series Mode Rejection: >66 db at 50 Hz ± 0.5% (or 60 Hz ± 0.5%).

A.C. Common Mode: $\geq$140 db at 50 Hz ± 0.5% (or 60 Hz ± 0.5%), measured with 1 kΩ unbalance in either lead; GUARD connected to Input Lo.

D.C. Common Mode: >140db, measured with 1 kΩ unbalance in either lead; guard connected to Input Lo.

NOTE: Series and common mode rejection for a.c. are defined as:

$$20 \log_{10} \frac{\text{a.c. signal (r.m.s. volts)}}{\text{Max error in readings (volts)}}$$

Common Mode Rejection specifications are maintained with any combination of options and are unaffected when grounded devices are used in conjunction with the BCD Output Unit SM 261.

Settling Time (to 0.005% of step input): 800 ms

Overload Limits: The maximum voltage which can be applied without damage:

Input Hi to Input Lo:	Direct ranges:	250 V d.c. or r.m.s. (1kV for $\geq$ 5sec).
	Attenuated ranges:	1.1 kV d.c. or peak a.c.
Input Lo to Guard:	$\leq$ 100 V d.c. or peak a.c.	
Guard to Chassis:	1.1 kV d.c. or peak a.c.	

Digitisation Time: 400 ms.

Reading Rate: 2.5 readings per second.

Display: 6 in line, side-view numerical indicator tubes with integral decimal points. 1 side view a.c./polarity indicator tube.

Temperature Range: Operational : 0°C to + 50°C.
Non-operational: − 40°C to +75°C.

Power Requirements:	(i)	Voltage ranges:	230 V, ± 15%, or 115 V, ± 15%.
	(ii)	Frequency range:	45 Hz to 66 Hz.
	(iii)	Power Consumption:	20 VA (approx.).
Dimensions:	(i)	Height (front Panel):	3½ in. (8.9 cm approx.).
	(ii)	Width (front Panel):	13 $^{1}/_{16}$ in. (33 cm approx.).
	(iii)	Depth:	11½ in. (29.2 cm approx.).
	(iv)	Weight:	13lb.(6 kg) approx, with options fitted.

2. DIGITAL VOLTMETER SM 214A

Specification as for SM 214, but with A.C. Voltage Boards SM 260 fitted, giving the voltmeter a.c. measurement facilities. SM260 can be purchased separately, if required.

A.C. Ranges (r.m.s.):	1.1 V	direct range.
	11V, 110V, 1.1 kV	attenuated ranges.
Input Impedance:	Direct Range:	100 MΩ in parallel with 60 pF.
	Attenuated Range:	1 MΩ ± 1% in parallel with 60 pF.
Maximum Resolution:	10 μV (on 1.1 V range).	
Accuracy (to full scale):		
90 days (+ 20°C to + 30°C):	20 Hz to 40 Hz:	± 0.5% of input, ± 0.02% of range.
	40 Hz to 10 kHz:	± 0.1% of input, ± 0.02% of range.
	10 kHz to 50 kHz:	± 0.5% of input, ± 0.02% of range.
Temperature Coefficient:		
0°C to + 20°C and +30°C to +50°C:	± 0.005% of input, ± 0.0005% of range per °C.	
Noise Rejection		
D.C. Common Mode Rejection:	> 140 dB, measured with 1 kΩ unbalance in either lead, Guard connected to Input Lo.	
A.C. Common Mode (at 50 Hz):	> 70 dB, measured with 1 kΩ unbalance in either lead, Guard connected to Input Lo.	
Settling Time (to 0.1% of step change):	< 2 seconds.	
Overload Limits:	Direct Range:	250 V r.m.s. at 50 Hz.
	Attenuated Ranges:	1.1 kV r.m.s.
	Input Voltage x frequency in Hz should not exceed 10^7.	

Superimposed D.C.	Direct Range:	± 250V d.c.
	Attenuated Ranges:	± 1.1 kV (peak a.c. + d.c. must not exceed ± 1.5 kV.)

3. DIGITAL VOLTMETER SM 214B

Specification as for SM 214, but fitted with the BCD Output Unit SM 261, to produce fully isolated parallel, buffered, outputs. The output logic levels are as for standard 7400 Series TTL. ***(See Section 3, Para. 5.2 for pin nos.).***

Logic 1:	+ 2.4 V to + 5V	
Logic 0:	0 to + 0.4V, 10 mA sink capability.	
Outputs:	5 full decades in BCD	20 lines
	Overrange digit:	1 line
	Polarity (logic 0 for negative)	1 line
	Range Information in BCD:	4 lines
	End of conversion (logic 1 for digitisation complete):	1 line
	End of ramp-up (logic 1 at end of the first cycle of the dual ramp conversion)	1 line
Inputs:	External Trip (logic 0 commands a single shot reading when the instrument is in the Hold mode. Contact closure is equivalent to logic 0).	1 line
	0V reference (digital ground):	1 line
Protection:	Incorrect connection of over-voltages to the BCD connector pins will not damage SM 214, although damage to SM 261 may occur.	
Isolation:	All common mode rejection specifications apply with SM 261 fitted.	

4. DIGITAL VOLTMETER SM 214/E

Specifications as for SM 214, but with 1 μV Amplifier Board SM 262 fitted, to give 1 μV sensitivity.

Maximum Resolution:	1 μV (on 110 mV d.c. range)
Accuracy of 110 mV range:	
24 Hours (+ 25°C, ± 1°C):	± 0.002% of input, ± 0.002% of range
90 days (+ 20°C to + 30°C):	± 0.007% of input, ± 0.003% of range
1 year (+ 20°C to + 30°C):	± 0.01% of input, ± 0.003% of range
Temperature Coefficient: 0°C to + 20°C and + 30°C to + 50°C:	0.0006% of input per °C
Temperature Coefficient of Zero:	0.2 μV per °C

Input Impedance:	> 100 M Ω
Overload Limit on 110 mV range:	Maximum voltage that can be continuously applied without damage is 100 V d.c. or r.m.s.

5. DIGITAL VOLTMETER SM 214/AB

Specification as for SM 214/A and SM 214/B

6. DIGITAL VOLTMETER SM 214/AE

Specification as for SM 214/A and SM 214/E

7. DIGITAL VOLTMETER SM 214/BE

Specification as for SM 214/B and SM 214/E

8. DIGITAL VOLTMETER SM 214/ABE

Specification as for SM 214/A, SM 214/B and SM 214/E

9. CURRENT SHUNT SET SM 263

Current Measurement:	A.C. or d.c.					
Output Voltage for Rated Current Range:	100 mV					
Current Ranges:	1A,	100mA,	10mA,	1mA,	100μA,	10μA
Resolution (SM 214E)	10μA,	1 μA	100nA	10nA	1nA	100 pA
Resolution (SM 214, SM 214/A, SM 214/B)	100μA	10μA	1μA	100nA	10nA	1nA

D.C. Accuracy:

Absolute:	All Ranges:	± 0.01%.
Temperature Coefficient:	1A Range: Other Ranges:	± 20 ppm per ^{o}C. ± 5 ppm per ^{o}C
Stability, per annum (+ 20^{o}C to + 30^{o}C):	All Ranges:	± 0.01%.

A.C. Accuracy:	There is no significant degradation in the accuracy of SM 214/A when used with the current shunt.

Dimension of each Shunt:	(i) Width:	2.4 in. (6.1 cm).
	(ii) Height:	0.82 in. (2.08 cm).
	(iii) Depth:	1.5 in. (3.81 cm).

SECTION 2

GENERAL INFORMATION

1. INTRODUCTION

1.1. The SM 214 Integrating Digital Voltmeter (fig. 2.1.) is a lightweight, all solid state instrument, incorporating MSI integrated circuits, providing high reliability. The instrument (in its most comprehensive form) is capable of d.c. and a.c. (voltage and current) measurements at a short term accuracy of 0.002% of reading, ± 0.002% of full scale, and has a full scale reading of 109999. The input is fully floating, made possible by incorporating an isolated power supply in the analogue section with interconnections made between that section and the digital section by miniature toroidal transformers. A drift correction system automatically ensures freedom from zero drift. Front panel offset controls can be adjusted to null small error voltages occurring in external circuitry, due to, for example, thermal e.m.f.'s.

2. MODELS AND FACILITIES

2.1. The SM 214 Digital Voltmeter is available in various versions as follows:-

(a) *SM 214.* This is the basic model, which has four d.c. voltage ranges and a maximum (best) resolution of 10 μV (on the 1.1V range). The display gives a steady, non-blinking readout. The a.c. ranges and the 110 mV d.c. range (although included on the range selector) are not operative on this model; the front panel terminals are open - circuit at these positions.

(b) *SM 214A.* This model has four d.c. voltage and four a.c. voltage ranges and a maximum (best) d.c. and a.c. resolution of 10 μV (on the 1.1V ranges). The a.c. ranges are provided by two, internally fitted, a.c. boards which can also be added to the basic SM 214 instrument, as a kit (Type No. SM 260).

(c) *SM 214B.* This model has four d.c. voltage ranges, a maximum (best) resolution of 10 μV (on the 1.1V range) and incorporates a buffered fully isolated parallel BCD output facility, suitable for driving a digital printer, for example. Connections are made via a 34-way connector on the rear panel. The BCD output facility is provided by the (internally fitted) BCD Outputs Unit SM 261, which is also available in kit form to convert the basic SM 214 instrument.

(d) *SM 214E.* This model has five d.c. voltage ranges, 110mV, 1.1V, 11V, 110V and 1.1 kV. On the 110 mV range, the maximum resolution is 1 μV. This increased resolution is provided by the (internally fitted) 1 μV Amplifier Board SM 262, which can also be supplied separately for addition to the basic SM 214 instrument. The four a.c. voltage ranges (although included on the range selector) are not operative on this model; the front panel terminals are open-circuit on these positions.

2.2. The facilities offered by the models described above can be combined.

(a) *SM 214AB.* This model is fitted with SM 260 and SM 261 options. It has four d.c. voltage and a.c. voltage ranges, a maximum resolution of 10 μV (on the 1.1V range) and the BCD output facility.

(b) *SM 214AE.* This model is fitted with SM 260 and SM 262 options. It has five d.c. voltage ranges with a maximum (best) resolution of 1 μV (on the 110 mV range) and four a.c. voltage ranges.

(c) *SM 214BE* This model is fitted with SM 261 and SM 262 options. It has five d.c. voltage ranges with a maximum (best) resolution of 1 μV (on the 110 mV range) and the BCD output facility.

FIG 2.1 DIGITAL VOLTMETER SM 214

(d) ***SM 214ABE.*** This model is fitted with SM 260, SM 261 and SM 262 options. It has five d.c. voltage ranges and four a.c. voltage ranges. The maximum (best) resolution is 1 μV (on the 110 mV d.c. range). The BCD Output facility is also incorporated on this model.

2.3. ***Current Shunt Set SM 263.*** In addition to the above facilities, a set of six current shunts can be used with any model of the SM 214 to measure direct current up to a maximum of 1 A. The ranges provided are, 10 μA, 100μA, 1 mA, 10 mA, 100 mA and 1 A.

2.4. On '/E' Versions, the maximum resolution is 100 pA (using the 10 μA shunt on the 110 mV d.c. range). On other versions, the maximum resoltuion is 1 nA (using the 10 μA shunt on the 1.1V range).

2.5. On '/A' versions, direct and alternating current up to a maximum of 1 A can be measured (ranges as above) to a maximum resolution of 1 nA (using the 10 μA shunt on the 1.1V range).

3. PRINCIPLES OF OPERATION

3.1. The method of digitisation employed in the instrument is the 'Dual Ramp' System, which offers many advantages over alternative methods. A simplified description of the system is given below.

3.2. A block diagram of the system is shown in figure 2.2. The conversion is initiated by a count of 000000 in the main counter. At the start of the conversion, solid state switch S1 is turned on, and S2 is turned off. The switches remain in this condition until the counter reaches 124000. The clock oscillator frequency is chosen to be 620 kHz so that with a count of 124000 this 'ramp-up' period is 200 ms. This is equal to 10 periods of 50 Hz line frequency (12 periods of 60 Hz) giving good rejection of superimposed a.c. signals at these frequencies.

3.3. At the end of the ramp up period, the counter is reset. Switch S1 is opened and switch S2 is closed so that the input of the ramp amplifier is now taken to a reference voltage of opposite polarity. The output of the ramp amplifier A1, during this period is shown in fig. 2.3.

3.4. The switches remain in this condition until the output of A1, as indicated by the detector amplifier A2, again reaches 0V, at which point, the contents of the display counter are transferred to the store. Since the whole of the charge accumulated on capacitor C during the 'ramp up' period has now been removed, the display store contains the required representation of the input voltage in terms of the reference voltage.

3.5. If we consider the charge on capacitor C at the beginning of 'ramp up' to be zero, then the charge at the end of this period is given by:

$$q = it = \frac{V_{in}}{R} \times 124{,}000\ T$$

where T is the period of the clock oscillator.

Since capacitor C is completely discharged during the ramp down period then:-

$$q = it = \frac{V_{ref}}{R} \times NT$$

therefore

$$\frac{V_{ref}}{R} \times NT = \frac{V_{in}}{R} \times 124000\ T$$

$$N = \frac{V_{in}}{V_{ref}} \times 124000$$

where N is the number displayed.

A count of 124,000 is chosen to allow a reference voltage of 12.4V to be used. Unlike the simple ramp system, long term variations in the integrator time constant or clock oscillator frequency do not lead to measurement errors.

3.6. The system described above provides for negative input voltages only, but the system lends itself well to bipolar operation. A polarity decision is made at the end of the 'ramp up' period and, at this time, the output of the detector amplifier is used to select a reference voltage of the required polarity.

4. DRIFT CORRECTION SYSTEM

4.1. Any current or voltage offsets at the input of the ramp amplifier A1, or any voltage offsets at the input of the detector amplifier A2, will lead to both ranging errors and zero errors. Errors due to current drift at the input of A1 are minimised by employing junction field effect transistors (FET'S) as the input stage to the amplifier. Errors due to voltage drift are avoided in both amplifiers by a system of drift correction which operates during the periods when the voltmeter is not digitising.

4.2. A block diagram of the system is shown in fig. 2.4. During the drift correction period, chopper S3 is ON, and choppers S1, S2 and S4 are OFF. In this condition, negative feedback is applied around both amplifiers in series and any offset voltage in amplifier A1 will be stored in capacitor C1. Since the output of amplifier A1 must be at a voltage equivalent to the offset in amplifier A2 then this offset will be stored on capacitor C. Choppers S1, S2 and S3 are FET switches, whilst S4 is a transistor used as an emitter switch. During the conversion period S3 is OFF and S4 is ON, thus removing the overall feedback.

4.3. An additional advantage resulting from this form of drift correction is that the integrator capacitor C is effectively discharged before the beginning of ramp up. In the absence of the drift correct system it would be necessary to incorporate a switch across capacitor C to ensure this.

5. INPUT AMPLIFIER

5.1. Since the input impedance of the system considered so far is equal to the value of the integrator resistor (fig. 2.2) and the resolution is 100 μV, it is necessary to precede the ramp amplifier by an input amplifier, both to increase the input impedance to > 5000 MΩ and to provide the required resolution of 10 μV.

5.2. The amplifier used in this series of digital voltmeters is a time shared, drift corrected, differential amplifier of the form shown in fig. 2.5. The amplifier is drift corrected from the end of ramp up until the start of the next measurement. It has a gain defined by $\frac{R2 + R1}{R2}$.

These precision resistors are switched by the range switch to give a gain of 10 for the 1.1V range and unity for the 11V range.

5.3. During the drift correct period choppers S5 & S8 are OFF, and choppers S6 & S7 are ON, storing the offset voltage of the amplifier on capacitor C2. During the conversion period S5 is ON and S6 and S7 are OFF, thus the amplifier operates normally with series feedback via capacitor C2 defining the gain. All four choppers are junction FET's as is the input stage of the amplifier providing very low input current and voltage drifts. R3 is high compared to (R1 + R2).

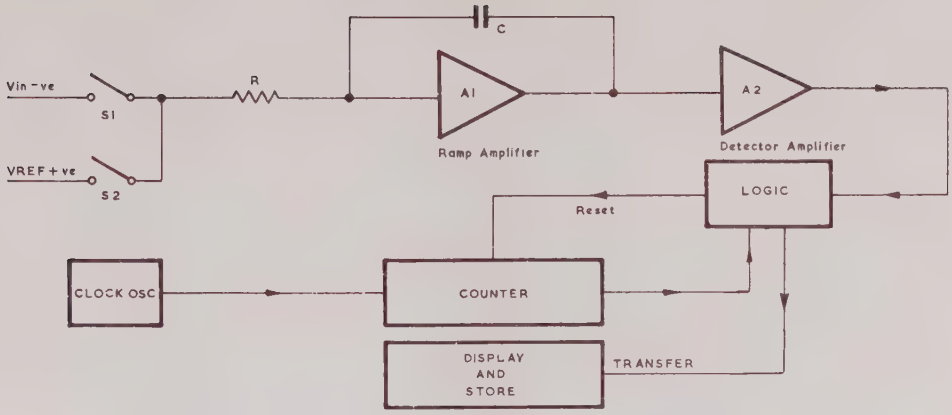


FIG. 2.2 DUAL RAMP SYSTEM

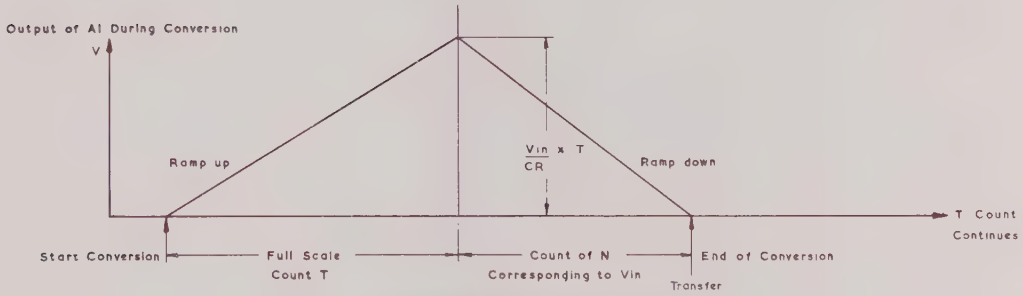


FIG. 2.3 RAMP AMPLIFIER OUTPUT

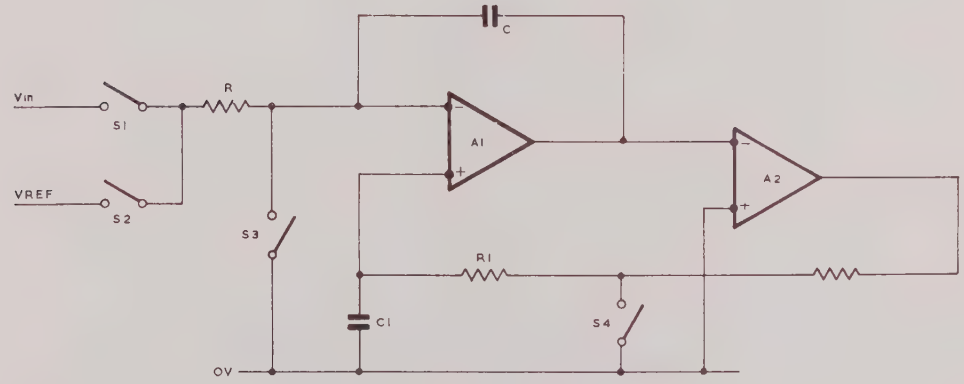


FIG. 2.4 DRIFT CORRECT SYSTEM

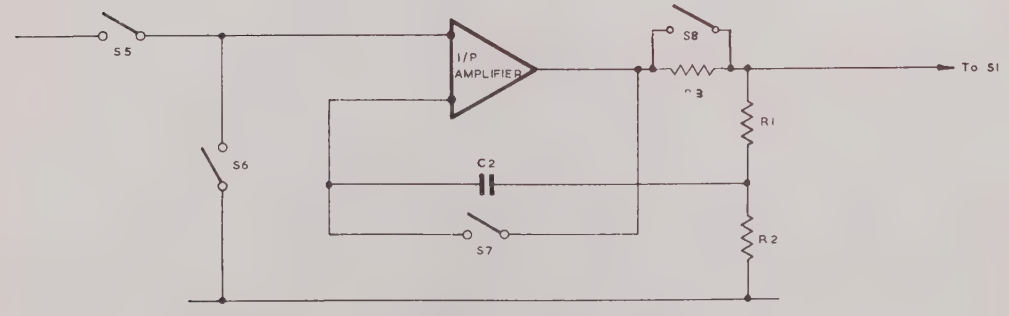


FIG. 2.5 INPUT AMPLIFIER

SECTION 3

INSTALLATION AND OPERATION

1. INTRODUCTION

1.1. This section contains all information necessary to install, operate and calibrate the instrument.

2. UNPACKING

2.1. The instrument is supplied sealed in a polythene bag and surrounded by rubber packing blocks. After removal, these should be retained for use again should further transit be required.

3. ACCESSORIES

3.1. The following items are available as accessories to the instrument:

(a) 3-wire input lead.

(b) Carrying Case SM 210/C.

(c) Rack Mounting Kit SM 210/R.

(d) Instruction Manual.

3.2. The following items can be added to the basic SM 214 instrument.

(a) Set of AC Plug-in boards (2-off) SM 260.

(b) BCD Outputs Unit Assembly Kit SM 261.

(c) 1 μV Plug-in Amplifier Board SM 262.

(d) Current Shunt Set SM 263, (set of 6 shunts).

4. POWER (MAINS) INPUT SELECTION

4.1. The digital voltmeter is normally supplied wired to accept a 230 V mains input. To alter the mains setting from 230 V to 115 V operation, the primary windings on the two mains transformers (main and floating power supplies) are reconnected in parallel as shown in fig. 3.1.

5. CONNECTIONS

5.1. Mains Input Lead. Connections are as follows:

Colour Code	Function
Brown	Live
Blue	Neutral
Green/Yellow	Earth

5.2. BCD Output Socket. Connections are as listed below. The logic levels are as for 7400 TTL logic:

Logic 1: + 2.4 V min. to +5 V max.
Logic 0: +0.4 V max, sink capability 10 mA.

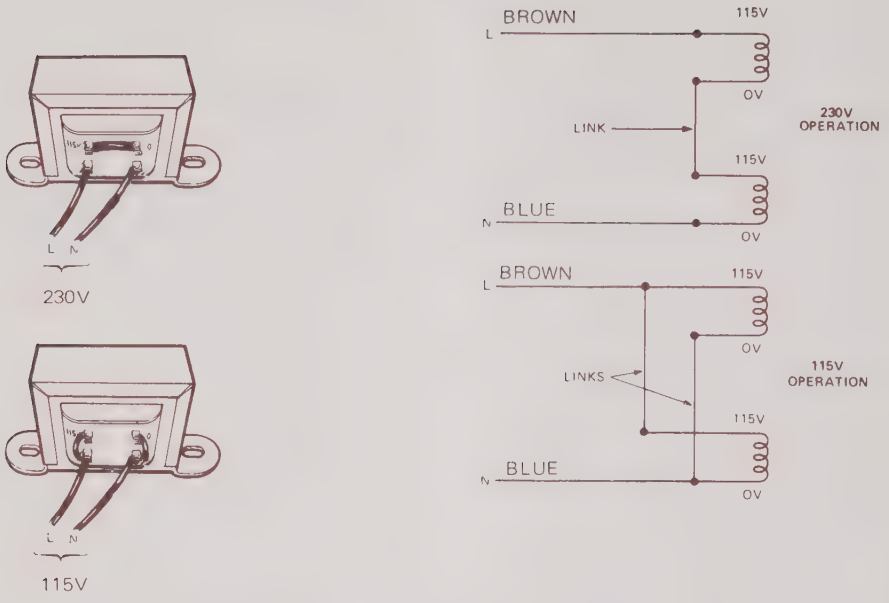


FIG 3.1 MAINS VOLTAGE SELECTION

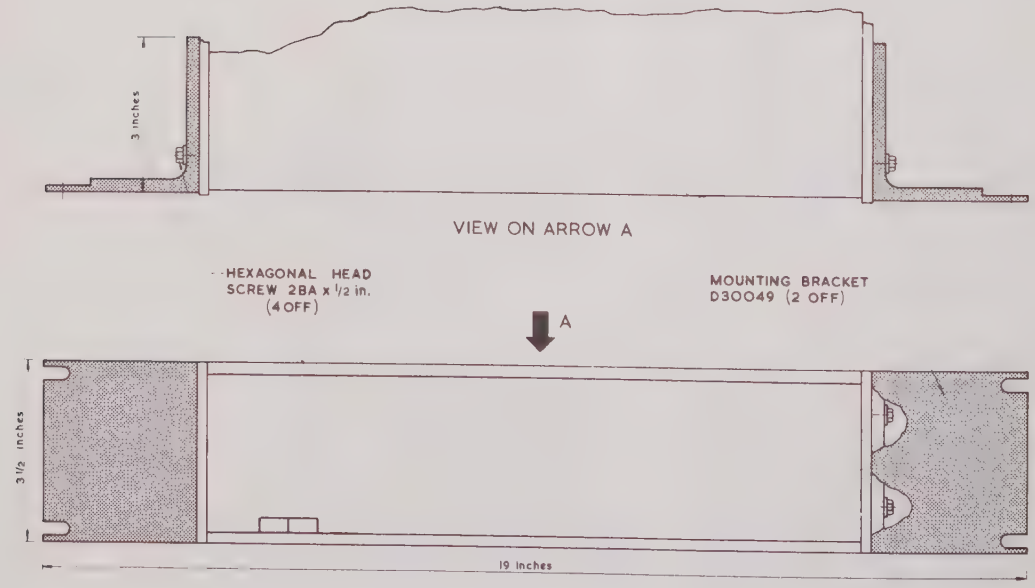


FIG 3.2 RACK MOUNTING KIT SM 210/R

Units	Tens	Hundreds	Thousands	Ten-Thousands	Hundred-Thousands	BCD O/P
A1	A2	A3	A4	A5	A6	1
B1	B2	B3	B4	B5	—	2
C1	C2	C3	C4	C5	—	4
D1	D2	D3	D4	D5	—	8

Function	Pin No.	Operational Logic State
Conversion Complete	C6	0 to logic 1.
End of Ramp-up	D6	Logic 1 at the end of the first cycle of the dual ramp conversion.
Polarity	B6	Logic 0 (+ve), Logic 1 (-ve).
External Trip Trigger Input	A8	Logic 0 input commands a single shot reading when instrument is in HOLD.
Range Output A	A7	See Table below.
Range Output B	B7	
Range Output C	C7	
Range Output D	D7	
OV (Digital ground)	B8	The instrument has separate analogue and digital grounds. Since the 0V (logic) line is grounded at the instrument, care should be taken to avoid large circulating currents when the instrument is connected to external equipment, sufficiently remote to give the possibility of significant differences in ground potentials. To avoid this, ensure that the system is grounded at ***one*** point only, either by removing the ground connection at the external equipment ***or*** at the instrument. If it is required that the instrument's chassis remains grounded, then it is necessary to remove an internal link. This should ***only*** be performed by a qualified service engineer and assitance can be obtained from ***Service Department, S.E. Laboratories (Engineering) Ltd., North Feltham Trading Estate, Feltham, Middlesex, England. Tel. No. 01-890-1166.***

RANGE OUTPUTS TRUTH TABLE

	Range Selected	Output D (pin D7)	Output C (pin C7)	Output B (pin B7)	Output A (pin A7)
d.c.	110 mV	0	0	0	0
	1.1V	0	0	0	1
	11V	0	0	1	0
	110V	0	0	1	1
	1.1kV	0	1	0	0

cont.

cont.

	Range Selected	Output D (pin D7)	Output C (pin C7)	Output B (pin B7)	Output A (pin A7)
a.c.	1.1 kV	0	1	0	1
	110V	0	1	1	0
	11V	0	1	1	1
	1.1V	1	0	0	0

6. RACK MOUNTING KIT (SM 210/R)

6.1. The instrument can be used on the bench or mounted in a standard 19th inch rack. Extensions are fitted to either sid of front panel as shown in fig. 3.2.

7: SUMMARY OF CONTROLS, CONNECTORS AND INDICATORS

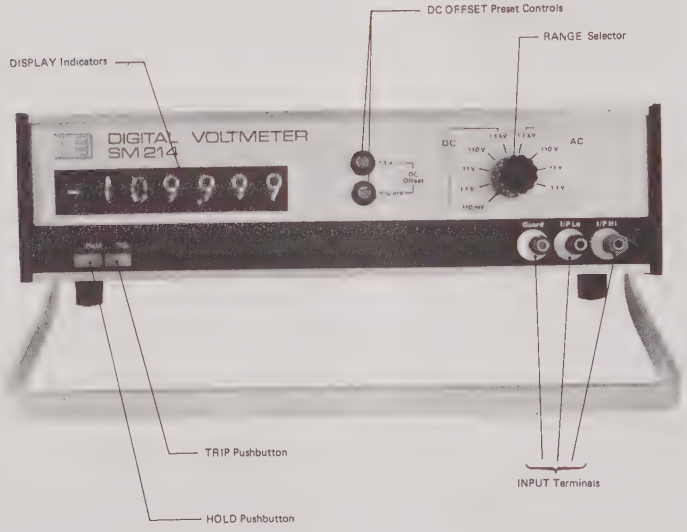


FIG. 3.3 CONTROLS, CONNECTORS AND INDICATORS

7.1. The front panel controls, connectors and indicators are identified as follows (fig.3.3):

(a) Display Indicators: 6-side view numerical indicators whch display a full scale reading of 109999. 1 side view polarity indicator displays + or — on d.c. measurements and ∿ on a.c. measurements.

(b) Range Selector:

A 9-position rotary switch as follows:

(a) D.C. Voltage Ranges:

Sw. Posn.	
1.	110 mV (SM 262 Fitted)
2.	1.1 V
3.	11 V
4.	110V
5.	1.1 kV

(b) A.C. Voltage Ranges (SM 260 fitted)

Sw. Posn.	
6.	1.1kV
7.	110V
8.	11 V
9.	1.1V

(c) DC OFFSET Preset Controls:

These are provided to null small external error voltages such as thermal e.m.f.'s:

(i) 110mV. Operational only on instruments fitted with the 1 μV Amplifier Board SM 262. The control is adjusted for a reading of ± 000000 on the 110 mV range with all three input terminals shorted.

(ii) 1.1V. Operational on all instruments and is adjusted for a reading of ± 000000 on the 1.1 V d.c. range, with all three input terminals shorted.

(d) HOLD push-button:

When pressed, the display is held at the last measurement taken.

(e) TRIP Push-button:

Used with the HOLD push-button pressed,to take single-shot readings.

(f) I/P Hi, I/P Lo terminals:

Connections for input voltage.

(g) GUARD Terminal:

Linked to I/P Lo for normal operation.

7.2. The controls and connectors on the rear panel are identified as follows:

(a) POWER ON Switch:

With this toggle switch set to ON, the numerical indicators should glow.

(b) BCD Output Socket:

34-way McMurdo socket provided when SM261 is fitted. Functions and connections are listed in Section 3, Para. 5.2.

(c) Mains Fuse:

(i) 230V mains: 250mA

(ii) 115V mains: 500mA

8. MEASUREMENT PROCEDURE

8.1. Switch-on

(a) Before switching on, the following preliminary checks should be made:

(i) Ensure that the instrument is correctly set for the local mains supply voltage (connected for 230V unless otherwise requested).

(ii) If the instrument has been in store for a prolonged period, as a precautionary measure, it should be inspected for evidence of dampness.

(b) Switch the POWER ON switch to ON. Check that the indicators tubes glow. To obtain the specified '1 year' accuracy (see Section 1) allow a 20 minute warm-up time to elapse. To obtain the specified '90 day' accuracy, allow a 1 hour warm-up time to elapse.

8.2. Setting DC OFFSET

8.2.1. The purpose of the DC offset controls is to null small, external, error voltages, such as thermal e.m.f's. Having switched on the instrument and allowed the required warm-up period to elapse (see Para. 8.1. (b) above):

(a) Set the Range Selector to the 1.1V d.c. range. Link together the I/P Hi, I/P Lo and GUARD terminals.

(b) Adjust the 1.1V DC OFFSET control for an indicated reading of ± 0.00000.

Additional steps for SM 214E

(c) Set the Range Selector to the 110 mV d.c. range.

(d) Adjust the 110 mV D.C. OFFSET control for an indicated reading of ± 000.000.

8.3. D.C. Voltage Measurement

(a) Check that the HOLD push-button is not depressed.

(b) Set the Range Selector to the 1.1 kV (d.c.) range.

(c) Connect the voltage-to-be-measured to the terminals marked I/P Hi and I/P Lo, with GUARD and I/P Lo Linked.

CAUTION

When the voltage value is unknown, it is always advisable to select the highest range and then 'range down', since each range is limited to a maximum overload voltage before damage occurs. These limits must be observed (see Table below):

DC Range Selected	Maximum Voltage	Across Terminals
110 mV	100 V d.c. or r.m.s.	I/P Hi to I/P Lo
1.1V	250 V d.c. or r.m.s.	I/P Hi to I/P Lo
11V	250 V d.c. or r.m.s.	I/P Hi to I/P Lo
110V	1.1 kV d.c. or peak a.c.	I/P Hi to I/P Lo
1.1 kV	1.1 kV d.c. or peak a.c.	I/P Hi to I/P Lo

(d) Switch the Range Selector down through the ranges until a reading of optimum resolution is obtained. If the indicated reading is 109999, this means that the input voltage has exceeded the full scale of the range selected and a less sensitive (higher) range should be selected.

8.4. D.C. Current Measurment using Current Shunt Set SM 263.

(a) Check that the HOLD push-button is not depressed.

(b) Select the 1 A current shunt and plug it into the I/P Hi, I/P Lo and GUARD terminals on the front panel.

(c) Set the Range Selector to:-

(i) 110 mV d.c. range on SM 214E

(ii) 1.1V d.c. range on SM 214

(d) Connect the current-to-be-measured to the shunt terminals. The instrument now displays current, 100mV representing 1 A.

(e) Having determined the approximate current value, select the current shunt most suitable for an accurate measurement.

The current ranges and resolutions are listed in the table below. The output voltage for a rated current range is 100 mV.

Current Range	SM 214E Resolution	SM 214 Resolution	Current Shunt Resistance
1 A	10 µA	100 µA	0.1Ω
100 mA	1µA	10 µA	1Ω
10mA	100nA	1µA	10Ω
1mA	10nA	100nA	100Ω
100µA	1nA	10nA	1kΩ
10µA	100pA	1nA	10kΩ

8.5. A.C. Voltage Measurement

NOTE: To obtain a.c. voltage measurements, option SM 260 must be fitted to the instrument.

(a) Check that the HOLD push-button is not depressed.

(b) Set the Range Selector to the 1.1 kV a.c. range.

(c) Connect the voltage-to-be-measured to the terminals marked I/P Hi and I/P Lo, with GUARD and I/P Lo linked.

CAUTION

When the voltage value is unknown, it is always advisable to select the highest range and then 'range down' since each range is limited to a maximum overload, voltage before damage occurs. These limits must be observed (see table below):

AC Range Selected	Maximum a.c. Voltage	Across Terminals
1.1V	250 V r.m.s. at 50 Hz	I/P Hi — to — I/P Lo
11V	1.1 kV r.m.s.	I/P Hi — to — I/P Lo
110V	1.1 kV r.m.s.	I/P Hi — to — I/P Lo
1.1kV	1.1kV r.m.s.	I/P Hi — to — I/P Lo

NOTE: The product of the r.m.s. input voltage amplitude and the frequency (in Hz) should not exceed 10^7 (Vin x Hz = $<10^7$).

When the a.c. voltage - to - be - measured is superimposed on a d.c. level, the overload limits are as shown in the table below (see also fig. 3.4).

A.C. Range Selected	V max.
1.1V	± 250V
11V	± 1.5kV
110V	± 1.5kV
1.1kV	± 1.5kV

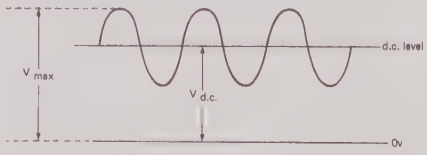


FIG. 3.4. A.C. VOLTAGE OVERLOAD LIMITS

NOTE: On fig 3.4, V d.c. (with no superimposed a.c.) should never exceed ±250 V (on 1.1 V AC range) or ± 1.5 kV (on 11V AC, 110V AC and 1.1 kV AC ranges).

(d) Switch the Range Selector down through the ranges until a reading of optimum resolution is is obtained. If the indicated reading is 109999, this means that the input voltage has exceeded the full scale of the range selected and a less sensitive (higher) range should be selected.

NOTE: The SM 260 is mean reading,r.m.s. calibrated. Therefore, there will be errors if distortion is present in the a.c. signal-to-be-measured. The extent of the errors will be dependent upon the order of the harmonic and its phase relation to the fundamental.

8.6. AC Current Measurement

NOTE: For a.c. current measurement, the instrument must incorporate option SM 260 and be used with current shunt set SM 263.

(a) Check that the HOLD push-button is not depressed.

(b) Select the 1A current shunt and plug it into the I/P Hi, I/P Lo and GUARD terminals on the front panel.

(c) Set the range selector to 1.1V AC range.

(d) Connect the current-to-be-measured to the shunt terminals. The instrument now displays current, 100 mV representing 1A.

(e) Having determined to approximate current value, select a current shunt most suitable for an accurate measurement.

The current ranges and resolutions are listed in the table below. The output voltage for a rated current range is 100mV.

Current Range	SM 214	Current Shunt Resistance
1A	100 µA	0.1 Ω
100mA	10µA	1Ω
10 mA	1µA	10 Ω
1mA	100nA	100Ω
100µA	10nA	1kΩ
10µA	1nA	10kΩ

8.7. Hold and Trip Facility

(a) To hold a reading, depress the HOLD Push-button. A single shot reading is obtained by depressing the TRIP push-button.

(b) To release the hold condition, depress the HOLD push-button (for a second time).

9. APPLICATION NOTES

9.1. Thermal E.M.F.'s

9.1.1. Care should be taken, particularly on the most sensitive range, that errors are not caused by thermally induced voltages due to junctions of dissimilar metals. For example, where crocodile clips are used, they should be made of copper and NOT steel. Steel could produce an error of 40 $\mu V/^{o}C$. Some types of resistor, particularly metal oxide resistors, can also generate high thermal e.m.f.'s.

9.2. Common Mode Rejection

9.2.1. In some applications both input terminals (Hi and Lo) may be driven by an a.c. voltage - normally at 50 Hz - with respect to earth. When an impedance is included in the INPUT Lo line, this can lead to errors. These will show up as random errors in the readings and are due to the voltage drop across the resistor produced by the current flowing through stray capacitances (Cs) to earth.

9.2.2. Errors due to common mode voltages can be greatly reduced by connecting the GUARD terminal directly to the source of the a.c. voltage, as shown in fig. 3.5. The guard terminal is internally connected to a screening box which completely surrounds the input analogue circuits, so that under these conditions the effective stray capacity (C's) to ground from INPUT Lo is much less than Cs. It follows that for best results the input lead should be a twin core screened cable, with the screen connected to GUARD.

9.3. Noise Rejection

9.3.1. Although the rejection by the instrument to super imposed a.c. signals is high ($>$ 66 db at 50 Hz ± 0.5% and 66 Hz ± 0.5%) It may be necessary to employ an additional external filter (fig. 3.6) when very large a.c. signals are present. The instrument's high input impedance means that high value resistors may be employed in the filter eliminating the need for large capacitors.

9.3.2. The example shown in fig. 3.6. would give an additional rejection of about 60 db at 50 Hz, increasing by 12 db per octave above this frequency, so an a.c. signal of 300 V would produce a reading error of 10 μV.

9.4. Input Current

9.4.1. A particular feature of the instrument is the very low input current to the voltmeter, a point which is seldom specified in other instruments. Although the maximum input current is specified at 50 pA, the input current is typically less than 20 pA and is stable at 1 pA for some time. The instrument can therefore be used to measure very low leakage currents.

9.4.2. An example of this is shown in fig. 3.7. where this leakage current 1_L of an N channel junction f.e.t. is being measured to a resolution of 1 pA with the instrument set to the 1.1V range.

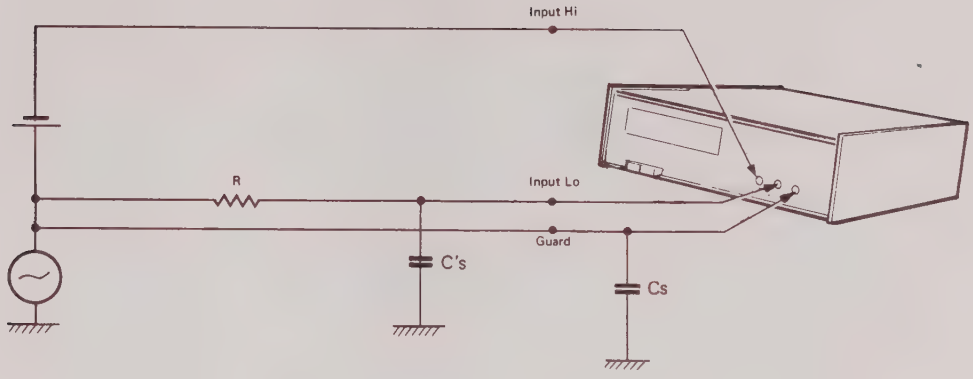


FIG 3.5 REDUCTION OF COMMON MODE ERRORS

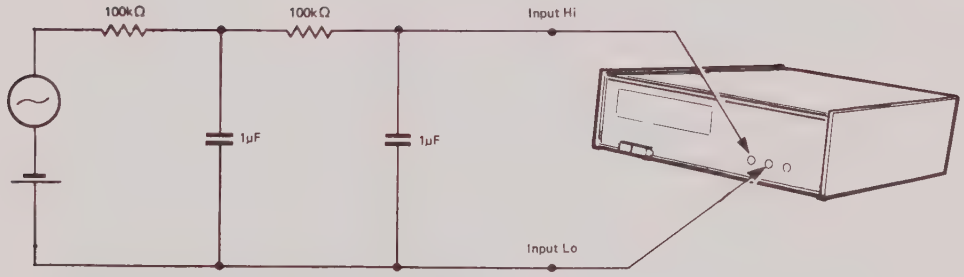


FIG 3.6 INCREASING THE REJECTION OF SUPERIMPOSED A.C. SIGNALS

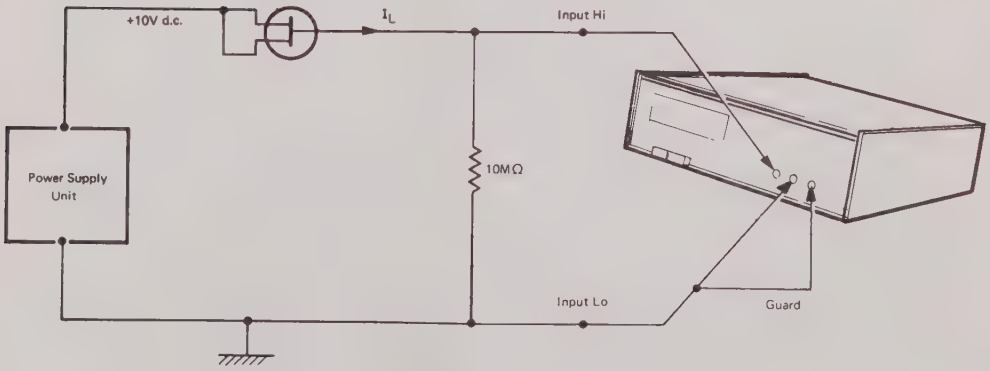


FIG 3.7 MEASUREMENT OF LOW LEAKAGE CURRENT

SECTION 4

CIRCUIT DESCRIPTION

1. INTRODUCTION

1.1 This section contains a detailed circuit description of Digital Voltmeter SM 214. The reader should be thoroughly conversant with the principle of operation employed in this instrument before attempting to study the information in this section. Reference should therefore be made to Section 2 of this manual, sub-sections 3, 4, 5 (pages 2.3 and 2.4).

1.2 Digital Voltmeter SM 214 can be considered as having two main sections, and each containing its own power supply:

(a) analogue section

(b) digital section

1.3 **Analogue Section.** This consists of a screening box in which are housed the sub-assemblies listed below.

(a) Mother p.c. board, into which are plugged:

(i) input amplifier board; this carries the overload protection neon, input filter, input amplifier and gain defining resistors together with FET choppers and associated drive circuits for drift correction,

(ii) floating logic board no 1; this carries the integrated circuit logic which provides the chopper drives for the input amplifier and floating logic (no 2) boards, together with constant current drives to the precision reference Zener diodes,

(iii) floating logic board no 2; this carries the 'ramp' amplifier and 'detect' amplifier with their associated FET choppers,

(iv) 1 μV amplifier board (SM 262); this is fitted on E versions only,

(v) a.c. attenuator board and a.c. converter board; these boards form the a.c. option SM 260 and are fitted on A versions only.

(b) Floating power supply board; this is mounted on the rear of the box and carries the precision Zener reference diodes.

(c) Heatsink assembly; this is also mounted on the rear of the box, and carries the integrated circuit regulators and rectifiers for the floating power supply board.

(d) Input attenuator; this is mounted on a separate tag board.

(e) Wafers C, D, E, F, G and H of the range switch SW1.

1.4 **Digital Section.** This section contains three units as listed below.

(a) Main logic and display board. This contains:

(i) counter, latch, decode and display circuits,

(ii) clock oscillator,

(iii) control logic,

(iv) range decode logic,

(v) toroidal transformer drivers and receivers

(b) BCD Outputs Unit SM 261; this is fitted on B versions only.

(c) Earthy power supply; this is mounted on the power supply chassis.

1.5 The digital section generates a reset pulse to the logic in the analogue section, at the beginning of the conversion, to ensure that the logic is in the correct state. This is followed by three trip pulses which drive the logic through the correct sequence for a conversion.

1.6 The first trip pulse initiates a conversion and corresponds to the start of the ramp up period (see fig 4.1.) After a count of 124.000 in the main counter a second trip pulse is generated which initiates the ramp down period.

1.7 When a detect signal is received from the analogue section, or the main counter reaches its full scale of 109999, a third trip pulse is generated corresponding to the end of conversion. At this point the contents of the main counter are transferred to the display stores and the result of the conversion is displayed.

1.8 The counter continues to run and the next conversion starts when the counter again reaches 124.000.

2. DIGITAL SECTION

2.1 Display and Logic Board

NOTE: The following description should be read in conjunction with the timing diagram fig 4.1.

2.1.1 Timing sequences are derived from the clock oscillator formed by the dual Schmitt trigger IC1, R28, C24, C25 and the 2.48MHz crystal. This output from this circuit is divided by IC2/9 to give a 1 24MHz clock train and again by IC2/12 to give the 620kHz input to the counter.

2.1.2 Immediately before a conversion, the inhibit transfer bistable IC17/12 is in the reset state and is inhibited, the detect bistable IC23/12 is inhibited, the latch IC30/6 and IC30/12 is at logic 0 on output 6 and the second trip pulse bistable IC27/12 is inhibited. IC8 is also inhibited.

2.1.3 A conversion is initiated by a count of 124,000 in the main counter when pin 6 of IC16/6 goes to logic 0, and IC16/8. Pin 8 goes to logic 1.

2.1.4 IC3/9 is clocked to logic 1 at a count of 124,004 by the output on pin 8 of IC16/8. This, in turn, steers bistable IC3/12 which is clocked to a logic 0 by the 1.24MHz clock, via gate IC4.3. The Q output of IC3/12 resets the counter. The $\overline{Q}$ output of IC3/12 provides the reset pulse to the analogue section via IC4/11, IC19/6 and the toroidal transformer driver TR6. It also resets the polarity latch IC31/8 and IC31/11 to a logic 1 on output pin 8 corresponding to negative polarity. IC3/12 resets IC39 and is therefore clocked to a logic 1 on the next edge of the 1.24MHz clock.

2.1.5 The logic 1 to logic 0 transition from $\overline{Q}$ IC3/12 is taken via gates IC4/11, IC19/6 and clocks the first trip pulse bistable IC27/9 to a logic 1. This generates the first trip pulse via IC30/8 and the toroidal transformer driver TR7. This transition also sets the latch IC30/6 and IC30/12 to a logic 1 on output pin 6, enabling the second trip bistable IC27/12, IC8 and the inhibit transfer bistable IC17/12. It also enables gate IC4/6.

2.1.6 At a count of 124.000 the output of gate IC16/6 goes to logic 0, clocking the second trip pulse bistable IC27/12 to a logic 1. The $\overline{Q}$ output of IC27/12 provides the second trip pulse, corresponding to the end of the ramp-up period, to the analogue section via gate IC30/8 and toroidal transformer driver TR7.

2.1.7 At a count of 124,004, IC16/6 output goes to logic 1 and IC16/8 output goes to logic 0. This clocks the inhibit transfer bistable IC17/12 to a logic 1 which enables the detect bistable IC23/12 and triggers the 'end ramp-up' monostable IC8. This produces a reset pulse to the counter, lasting approximately 10μs via gate IC4/3.

2.1.8 This delay between the start of ramp-down and the start of the counter is compensated by an equivalent delay in the analogue section. The purpose is to eliminate slight non-linearities at low readings.

2.1.9 A reset pulse is generated by IC3/9 and 12 but this is inhibited by gate IC4/11.

2.1.10 The logic 0 transition from IC16/8 generates an end-ramp-up signal for the BCD output board (SM 261) via IC4/6.

2.1.11 Following the second trip pulse(denoting the end of ramp-up) the analogue section generates a polarity signal to the polarity latch IC31/8 and IC31/11 via the transformer receiver TR4. This is a negative going pulse (to logic 0) at IC31/11 (input 13) for positive polarity. For negative polarity there is no pulse and the latch remains in the reset condition.

2.1.12 The conversion ends either when a 'detect' signal is generated by the analogue section or a full scale of 109999 is reached by the counter. If a detect signal is generated, this clocks the detect bistable IC23/12 to a logic 1 via the transformer receiver TR1, IC19/8 and IC15/13. If no detect pulse is generated, the bistable is clocked by the signal from the full scale detect gates IC18/8 and IC15/10 via IC15/13.

2.1.13 IC23/12 steers IC23/9, which is clocked to a logic 0 on the next 1.24MHz clock edge. IC23/9 then resets IC23/12, so that it is clocked back to a logic 1 on the following clock edge.

2.1.14 The third trip pulse and transfer pulse bistable IC23/9 generates the third trip pulse (denoting the end of ramp-down) which is fed to the analogue section via IC30/8 and the transformer driver TR7. It also generates the transfer pulse to the display latches via IC32/11 and TR5. The latch IC30/6 and IC30/12 is reset to its initial condition, logic 0 on output pin 6, and IC8 is inhibited by the logic 1 from IC30/12.

2.1.15 The output from IC32/11 also generates the conversion complete signal. This is fed to the BCD output board (SM 261) via the latch IC31/6 and IC31/3.

2.1.16 When the HOLD push-button is depressed the transfer pulse is inhibited by a logic 0 on input 12 of IC32/11 from the 'hold' bistable IC28/9. This is normally in the reset state.

2.1.17 When the push-button is operated the 'hold' bistable is tripped to a logic 1 via latch IC32/3 and IC32/6 and gate IC15/1. This allows one transfer pulse to reach the display latches via IC32/8, before the hold bistable is again reset by the trailing edge of the last trip pulse.

2.1.18 A conversion can also be initiated by an external trip pulse (logic 1 to logic 0 transition). This is applied via the rear panel 34-way connector, BCD output board (SM 261) and IC4 to IC15/1, input pin 3.

2.1.19 Range information from the range switch (in 1 of n code) is decoded to BCD code by, IC34/8, IC35/6 and IC35/8. It is then taken to the BCD output board (SM 261).

2.1.20 Where an a.c. range is selected, IC34/6 output is at logic 1. This is taken via the latch IC29 to the decoder IC33. This drives the AC sign of the polarity indicator tube V7.

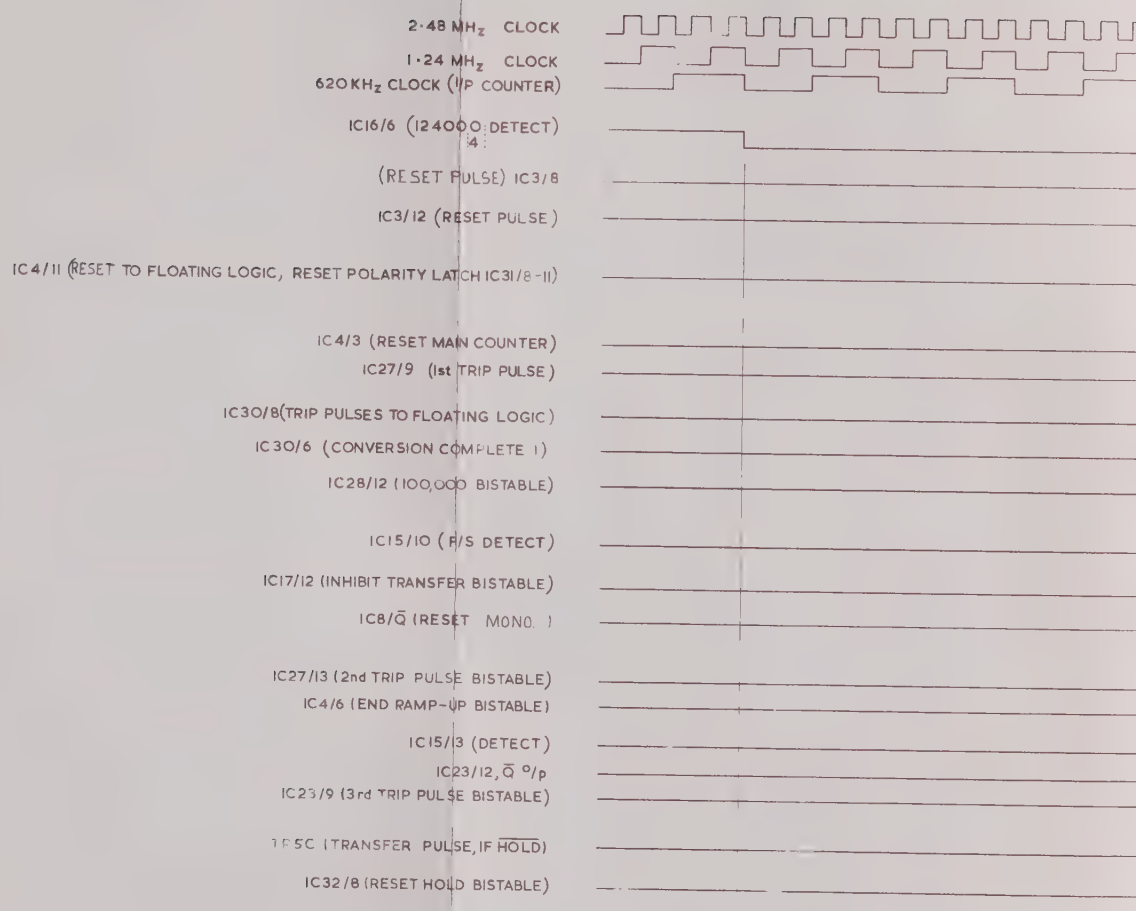
2.2 BCD Outputs Unit (Option SM 261)

2.2.1 This unit consists of the BCD output board and its associated cable form and rear panel connector. All digital inputs and outputs are buffered by the BCD board. The outputs handled by this board are as follows:

(a) five decoders of BCD, buffered by ICs 6/11, 6/3, 7/8, 6/6, 5/11, 5/3, 6/8, 5/6, 4/11, 4/3, 5/8, 4/6, 3/11, 3/3, 4/8, 3/6, 2/8, 2/6, 3/8 and 2/3.

(b) Overrange digit (100,000), buffered by IC 2/11.

(c) polarity output information, buffered by IC 1/12 (logic 1 for negative, logic 0 for positive),



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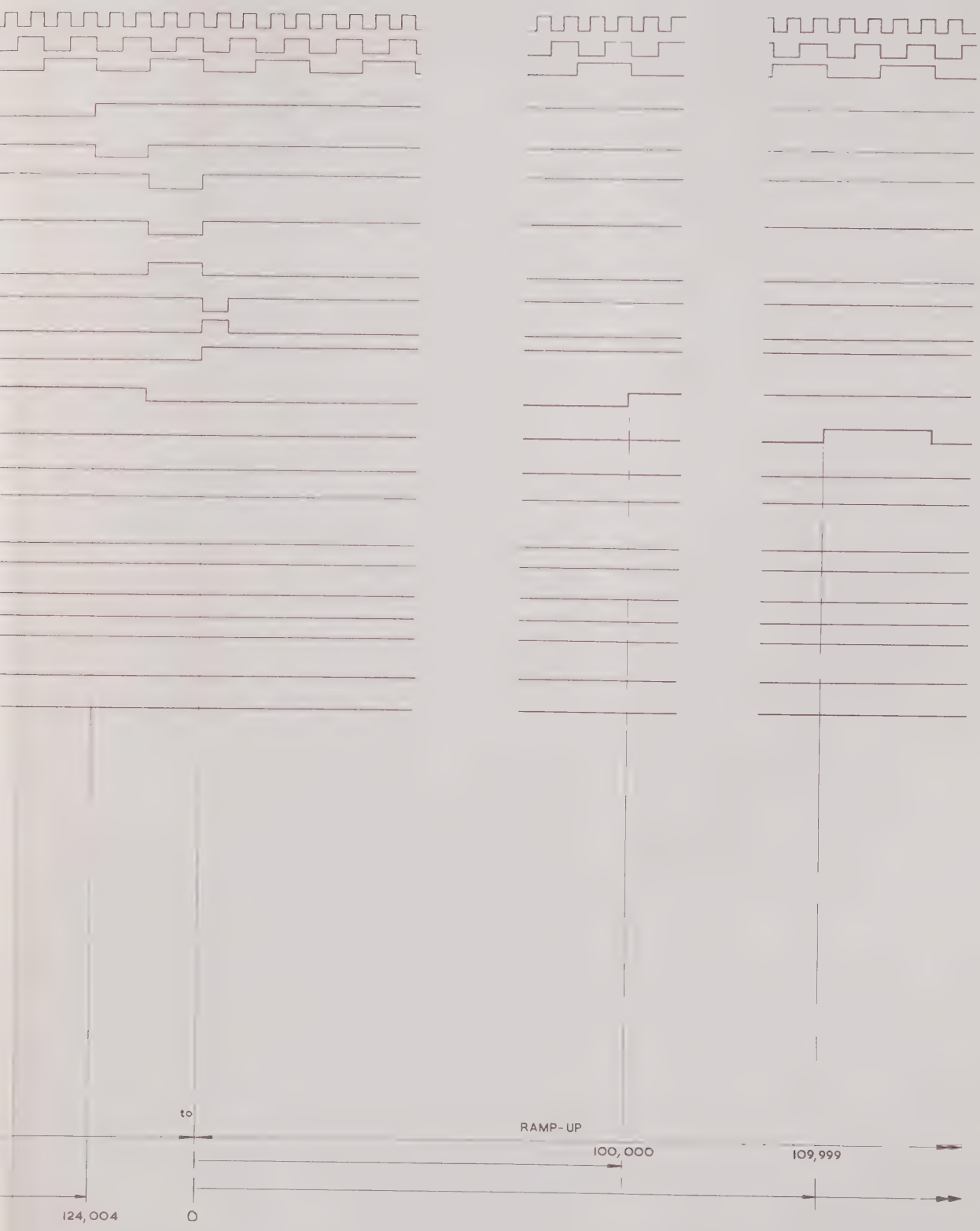
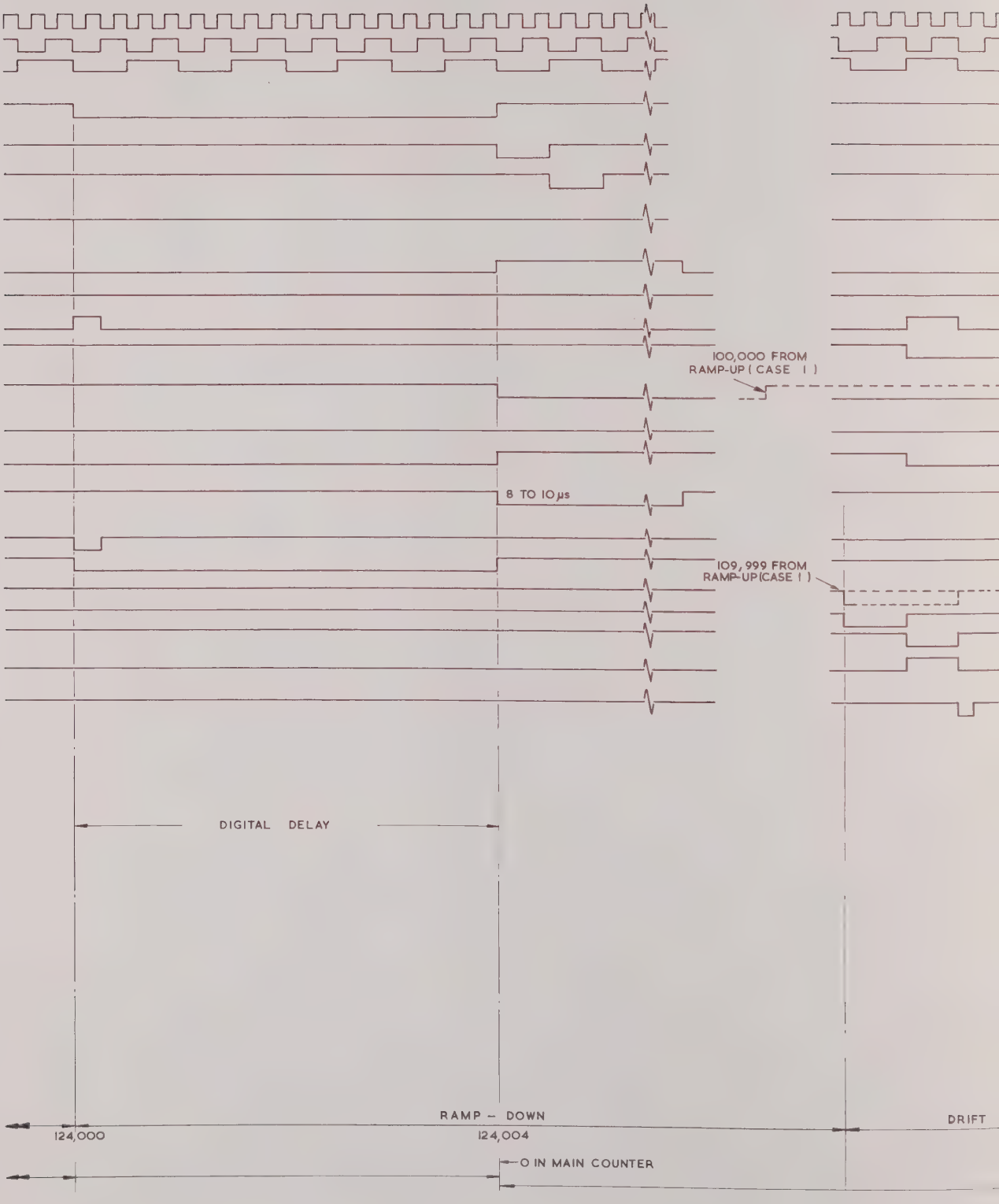
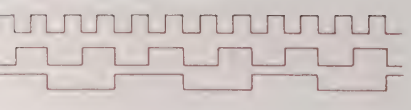


SHEET 1



SHEET 2

FIG 4.1 TIMING DIAGRAM



2·48 MH_z CLOCK

1·24 MH_z CLOCK

620 KH_z CLOCK (1/p COUNTER)

IC16/6 (124000 DETECT)

IC3/8 (RESET PULSE)

IC3/12 (RESET PULSE)

IC4/11 (RESET TO FLOATING LOGIC, RESET POLARITY LATCH IC31/

IC4/3 (RESET MAIN COUNTER)

IC27/9 (1st TRIP PULSE)

IC30/8 (TRIP PULSES TO FLOATING LOGIC)

IC30/6 (CONVERSION COMPLETE 1)

100,000 FROM RAMP-UP (CASE 2) → IC28/12 (100,000 BISTABLE)

IC15/10 (F/S DETECT)

IC17/12 (INHIBIT TRANSFER BISTABLE)

IC8/$\bar{Q}$ (RESET MONO.)

IC27/13 (2nd TRIP PULSE BISTABLE)

IC4/6 (END RAMP-UP BISTABLE)

IC15/13 (DETECT)

IC23/12 $\bar{Q}$ o/p

IC23/9 (3rd TRIP PULSE BISTABLE)

TRSC (TRANSFER PULSE, IF $\overline{HOLD}$)

IC32/8 (RESET HOLD BISTABLE)

RECT PERIOD

RECOMMENCES ON SHEET 1.

(d) four lines of range output information in BCD code, buffered by ICs 7/3, 7/6, 7/11 and 1/10. The range output code is shown in the table below.

Range	D7	C7	B7	A7
1	0	0	0	0
2	0	0	0	1
3	0	0	1	0
4	0	0	1	1
5	0	1	0	0
6	0	1	0	1
7	0	1	1	0
8	0	1	1	1
9	1	0	0	0

2.2.2 The end-ramp-up signal is buffered by IC1/8. This goes to a logic 1 at the end of the ramp-up period, remaining high for approximately 3μs

2.2.3 The end conversion signal is buffered by IC1/2. This signal is at logic 0 during the conversion and logic 1 between the end of conversion and the start of the next reading. It remains at logic 0 throughout when the HOLD push-button is operated.

2.2.4 The external trip input is buffered by IC1/6 and IC1/4. A logic 1 to logic 0 allows one transfer pulse to reach the display and output latches.

2.2.5 The fuse FS1 and D(Z)1 are included to limit any damage, due to accidental over voltages applied to any line externally, to the BCD board only.

2.3 Earthy Power Supply

2.3.1 The power supply generates a +5V supply for the earthy logic and a high voltage supply for the indicators tubes.

2.3.2 The +5V supply is rectified by the bridge rectifier D1 with C1 as reservoir capacitor. The output is stabilised by the integrated circuit regulator IC1.

2.3.3 The tube supply is half wave rectified by diode D2 and is +250V peak without smoothing.

3. ANALOGUE SECTION

NOTE: The following paragraphs describe the operation of the analogue section of the basic d.c. version of the SM 214. The 1μV Amplifier Board (option SM 262) and the AC Converter and Attenuator (option SM 260) are considered separately, in sub-sections 3.5 and 3.6 respectively.

3.1 Input Logic

3.1.1 The input logic is carried on floating logic board no 1 and is driven from the digital section via two windings of the double toroidal pulse transformers T4 and T5. The input logic transmits polarity information and a 'detect end of ramp-down' signal to the digital section via the other two windings of T4 and T5. The toroidal pulse transformers provide total isolation between the digital section and the analogue section. The input logic also generates all necessary drives to the choppers in the analogue section.

3.1.2 At the start of the conversion, the four bistables ICs 4/9, 4/12, 5/9 and 5/12 are reset to zero by TR28, driven from the digital section. The three consecutive trip pulses from the digital section fed via TR26, drive bistables ICs4/9, 4/12 and 5/12, through the following states:

Bistable	IC4/9 state	IC4/12 state	IC5/12 state
Reset	0	0	0
After 1st Trip Pulse	1	0	1
		Ramp-up period	
After 2nd Trip Pulse	0	1	1
		Ramp-down period	
After 3rd Trip Pulse	0	0	0
		Drift correct period	

3.1.3 Bistable IC5 is the polarity bistable and is clocked by the $\overline{Q}$ output of IC4/9 as the bistable goes to logic 0, at the end of ramp up, via IC6/11 and IC6/8. The polarity bistable is steered from the output of the detector amplifier, IC1 on floating logic board no 2, via TR27 and IC7/6. It is clocked to a logic 1, denoting positive polarity, if the output of IC1 is positive at the end of ramp up, and to a logic 0 if the output is low.

3.1.4 A logic 0 to logic 1 transition of IC5/9 generates a polarity pulse for the digital section, fed out via transformer driver TR25.

3.1.5 IC4/9 provides the necessary chopper drive to the input amplifier board. This is at logic 1 during the ramp-up period.

3.1.6 IC5/12 provides the chopper drive to the ramp and detector amplifiers on floating logic board no 2. This signal is high during both the ramp-up and ramp-down periods.

3.1.7 The drive to the reference choppers, which are turned on during the ramp down period, is provided by IC4/12. The drive is gated from the polarity bistable IC5/9 by IC7/11 and IC7/8. IC7/11 output is low during ramp-down for positive polarity and IC7/8 output is low for negative polarity.

3.1.8 IC4/12 also enables gates IC8/12 and IC8/6 during ramp-down, so that a detect pulse for the digital section can be generated. For positive polarity, gate IC8/12 is enabled by the polarity bistable IC5/9 and for negative polarity, IC8/6. Therefore, for a positive polarity the detect pulse is generated by a logic 0 to 1 transition at the collector of TR27 via IC8/12, IC8/8 and the transformer driver TR24. For a negative polarity, it is generated by a logic 0 to 1 transition at the output of gate IC7/6, (a logic 1 to 0 transition at TR27, via IC8/6, IC8/8 and TR24).

3.2 **Input Amplifier and Associated Circuits**

3.2.1 The purpose of the input amplifier is to provide a high input impedance, low drift buffer of accurately defined gain. The gain is selected by the front panel range switch to be either 1 or 10.

3.2.2 The input voltage-to-be-measured is applied between the front panel I/P Hi and I/P Lo terminals and taken via the toroidal transformer T3 to wafer SW1G of the range switch. T3 is included to eliminate problems due to mains source interference on rapid transients on the input lines.

3.2.3 On the 1.1V and 11V ranges, the input is switched directly to the input of the input amplifier on pin 3 via SW1G, R1 and SW1E. On the 110V and 1.1kV ranges the input is attenuated by 100:1 by the precision attenuator consisting of R3, R4, R5, R6, R7 and RV1 mounted on the filter board. The input voltage is taken to the attenuator via SW1G and from the attenuator to the amplifier input via SW1E.

3.2.4 The neon ILP1 provides over voltage protection since it limits at approximately 70V. Resistors R1, R8 and capacitor C2 form a low-pass filter to improve the rejection of superimposed a.c. voltages.

3.2.5 The input amplifier is drift corrected to I/P Lo during the ramp-down period and during the drift correct period. During drift correct, the chopper drive input at pin 11 is at logic 0. The states of the choppers are as follows:

TR4	TR5	TR8	TR10	TR12
off	on	on	off	off

3.2.6 The chopper drive turns TR1 off which turns TR2 off, thus turning chopper TR5 on. The source of TR5 is taken via pin 6, SW1C and pin 4 to R11 which is connected to signal earth. A small offset voltage of ±70μV is applied to R11 from the front panel 1.1V d.c. offset potentiometer via R61. The input of the amplifier is therefore referenced to signal earth (I/P lo) plus a small, variable offset voltage, during the drift correct period.

3.2.7 TR3 is turned on by TR2, turning off chopper TR4 via D5. I/P high is therefore isolated during drift correct. Transistors TR10 and TR12 are also turned off during drift correct by TR3 via D6 and D7. Transistors TR8 is turned on by TR2 via R23.

3.2.8 Depending upon the position of the range switch, SW1, capacitor C4 is connected to either pin 9 via pin 2 and SW1D, or pin 5. It is therefore taken to signal earth either via RV4 and R29 where a gain of 10 is selected, or R28, RV4 and R29 for unity gain. As negative feedback is applied around the amplifier 0A1 via TR8 and R18 to C4, any offset voltages are stored on the capacitor C4.

3.2.9 Since a small proportion of the offset voltage is applied to the other side of C4 (via R24 and pin 5 on 9), the zero offset potentiometer RV3 retains the small amount of control needed to null offset voltages elsewhere in the system. The attenuation is approximately 500 to 1 at a gain of 10 and 50 to 1 at unity gain.

3.2.10 During the ramp-up period, the states of the choppers are as follows:

TR4	TR5	TR8	TR10	TR12
on	off	off	on	on

3.2.11 TR6 is a source follower driven by the input voltage, with current set by the constant current source TR7. It drives the emitter follower TR9 which is supplied by constant current source TR11. The purpose of this circuit is to limit the maximum positive excursion of the drive to chopper TR4. The value of resistor R17 is chosen so that the minimum gate source voltage is about −1.0V.

3.2.12 During the ramp-up period, the amplifier operates as a voltage follower with feedback via pin 5, pin 2 and C4, on the 11V and 1.1kV ranges defining a gain of unity. Resistor R24 is by-passed by chopper TR10. On the 1.1V and 110V ranges, a gain of 10 is defined by feedback via pin 9, pin 2 and C4 from the precision resistor network R28, R33, RV4 and R29. The output of the input amplifier, during the ramp up period, is taken to the integrator on floating logic board no 2 via chopper TR12 and pin 10. The output voltage waveform before TR12 at pin 5 is shown below.

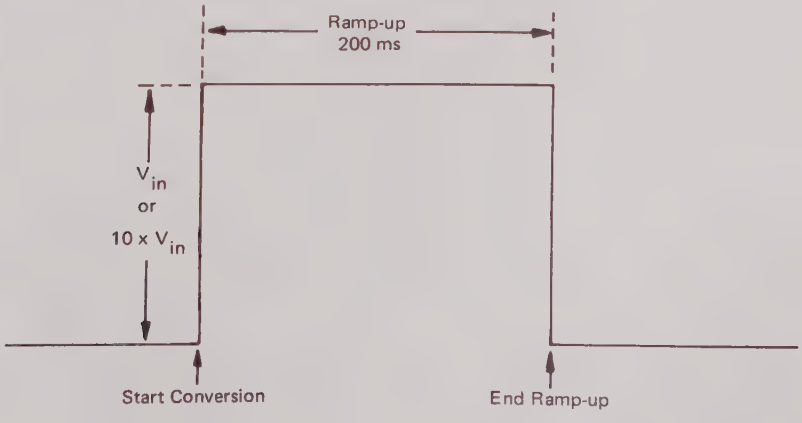


FIG. 4.2. AMPLIFIER O/P WAVEFORM (PIN 5)

3.3. **Integrator and Detect Amplifiers (floating logic board no.2)**

3.3.1 The integrator amplifier 0A2 and detector amplifier IC1 are drift corrected when the unit is not converting. For this condition the states of the choppers are as follows:

TR20	TR22	TR13	TR16
off	off	on	off

Transistors TR20 and TR22 are mounted on floating logic board no. 1.

3.3.2 The two amplifiers are connected in series, 0A1 driving the emitter follower TR15, with associated constant current source TR17. This, in turn, drives IC1 via R47. In the drift correct period, feedback is applied via R58, D8 and D9 to capacitor C6. Any offsets in 0A2 are stored on C6. Offsets in IC1 are stored on the ramp capacitor C8.

3.3.3 When the system is not operating in drift correct, the chopper TR13 is turned off and TR16 is turned on. Chopper drive from floating logic board no 1 is fed via pin 1 and TR14.

3.3.4 During the ramp-up period, the input to the integrator is fed via TR12 on the input amplifier board, pin 6, R34 (if fitted), RV5 and R39. A 'select-on-test' resistor (R34 or R35) is fitted as required calibration. Feedback to the integrator is applied initially via C8. As the output voltage at TP5 rises, D10, or D11, depending on the polarity of the input voltage, begins to conduct. The junction of D12 and D13 is at 0V so that conduction occurs at $\pm$0.6V approximately. Assuming a negative input voltage D11 conducts, D13 conducts and D14 conducts. Diodes D12 and D15 are reversed biased. Feedback is now applied via C8 and C11 in parallel. Since the value of C11 is approximately thirteen times C8, the slope of the ramp is reduced by this factor.

3.3.5 At the end of the ramp-up period, chopper TR12, on the input amplifier board, is turned off, and the ramp-down period starts. The input logic selects the correct polarity reference chopper drive as described in Paras 3.1 onwards. For a negative polarity input voltage TR20 is turned on via R63 and TR19.The input to the integrator is, therefore, taken to the positive reference voltage derived from the precision temperature compensated Zener diodes D(Z)21 and D(Z)23. The constant current supply to the diodes is described in Par. 3.4.1.The output of the integrator ramps downwards, towards 0V. As the output voltage approaches +0.6V, diode D11 starts to cut-off and feedback is again applied via C8 only. The rate of change is therefore increased by a factor of thirteen as the ramp approaches 0V. This has the effect of reducing the significance of noise at the input to the detector amplifier by the same factor, thus making it much less critical in this respect.

3.3.6 As the output of the integrator crosses 0V, the detector amplifier changes state causing the input logic to generate a detect pulse, completing the conversion.

3.3.7 Operation for positive input voltages follow the same sequence. The negative reference voltage, derived from DZ20 and DZ22, is applied to the integrator amplifier via chopper TR22. Transistor TR22 is driven from TR18 and TR23.

3.3.8 The output waveform of the integrator amplifier is shown below.

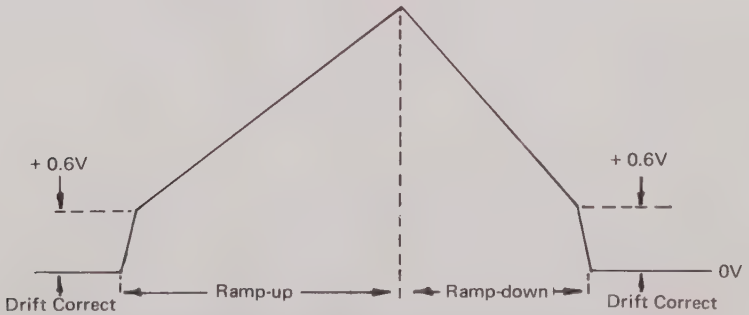


FIG. 4.3. INTEGRATOR O/P (TP5) FOR NEGATIVE I/P VOLTAGES

3.3.9 The reference voltage is modified by an amount proportional to the output of the integrator amplifier by resistors R48, R71 and R72. This introduces a small non-linearity cancelling out non-linearities due to dielectric absorption in the integrator capacitor C11.

3.3.10 At the start of the ramp down period, a small voltage is introduced at the input of the detector amplifier via R56 and RV6. This is of the same polarity as the reference voltage and, together with a digital delay in the main logic section, avoids slight non-linearities at low readings.

3.4 **Reference Voltage Generators (Floating logic board no 1)**

3.4.1 The two reference voltages are derived from the precision temperature compensated Zener reference diodes D(Z)20, D(Z)22, D(Z)21, D(Z)23. These are supplied from two constant current sources. IC2 provides the constant current to the positive reference diodes D(Z)21 and D(Z)23. These are mounted on the floating power supply board. The feedback ensures that the voltage at the junction of precision resistors R65 and R66 is equal to the positive reference voltages, plus defining the voltage at the amplifier output. The precision resistor R68 therefore defines the zener current. This resistor is selected on test and is chosen to optimise the current for each pair of Zener diodes to give a minimum temperature coefficient. This is typically less than 1ppm/^{O}C.

3.4.2 The negative reference voltage is generated in a similar way from D(Z)20 and D(Z)22 by amplifier IC3 with the select-on-test resistor R75.

3.5 **1μV Amplifier Board (Option SM 262)**

3.5.1 This board is fitted in E versions only. It provides an accurately defined gain of 10 from a low noise, chopper amplifier and is employed on the 110mV range only. On all other ranges it is switched out of circuit, and the amplifier input is taken to 0V via switch wafer SW1H.

3.5.2 When the 110mV range is selected I/P Hi is taken to pin 2 of the 1μV amplifier board via switch wafer SW1G. Resistor R8 and low leakage diodes D1 and D2 provide over-voltage protection up to a maximum of 100V.

3.5.3 Negative feedback from the precision resistor network R1, RV1 and R3 accurately defines a gain of 10.

3.5.4 The current zero, which does not normally require adjustment is by potentiometer RV2 and the select-on-test resistor R5. Voltage zero is adjusted by the 110mV DC offset potentiometer RV8 on the front panel. It should be noted that all versions of the SM 214 have a 110mV range position, but this range is inoperative if the SM 262 option is not fitted. A dummy board is fitted in place of the SM 262 option which connects the input of the input amplifier board to I/P Lo when this range is selected. I/P Hi is open circuit.

3.6 **AC Convertor and AC Attenuator Boards (Option SM 260)**

3.6.1 These boards are fitted to A versions only and together provide a mean reading, r.m.s. calibrated a.c. capability with a maximum resolution of 10μV.

3.6.2 On the 1.1kV, 110V, 11V and 1.1V a.c. ranges the input high line is switched to the a.c. attenuator board via SW1G. On the 1.1V a.c. range input high is then taken directly to the output, pin 8, of the a.c. attenuator board via reed relay RL1. This is energised by SW1F of the range switch. On the 11V a.c. range, input high is taken via the precision 10 to 1 attenuator formed by R5, R6 and RV3 and relay RL2. This is again energised from SW1F. The variable capacitor C5 and fixed capacitor C6 provide a.c. compensation at high frequencies. On the 110V and 1.1kV ranges, the operation is similar, the attenuation factors being 1000:1 and 100:1 respectively.

3.6.3 The output of the a.c. attenuator board is taken directly to the input, pin 1, of the a.c. connector board. The output of the a.c. convertor board is differential, output low being pin 6 and output high pin 5, and is not referenced to signal earth. On all a.c. ranges, therefore, the drift correct shunt chopper TR5 (input amp board) is switched not to R11 which is close to signal earth, but to the output lo of the a.c. convertor board. This means that the input amplifier is drift corrected to this voltage rather than signal earth and that the voltage measured is that between output high and output low. The chopper is switched by SW1C of the range switch.

3.6.4 The input is a.c. coupled by C1 and taken to the FET amplifier input via the overvoltage protection circuit D1, D2 and R1. The amplifier consists of an FET input stage TR1 and TR2, driven by the constant current source TR7, followed by the long tailed pair TR3 and TR4. These, in turn, drive TR5 and the output stage TR6. The amplifier is stabilised by d.c. feedback applied via R18, RV1 and R26, decoupled by C7. AC feedback is applied via D7 and R21 for negative half cycles and D8 and R23 for positive half cycles. Feedback ensures that the voltage on TR1 gate is equal to the input voltage. C2, R4 and R5 provide a degree of positive feedback to give a high input impedance. The gain of the amplifier to a.c. is defined by the precision resistors R21, R23, R26 and RV1.

3.6.5 The output voltage is filtered to remove the a.c. component by the two pole filter R20, C11, R22 and C13 on the output high line and by the three pole filter R24, C12, R25, C14, R29 and C16 on the output low line. Output high is negative with respect to 0V and output low is positive.

3.6.6 The advantage of this system, with differential output, is that any voltage drift at the input of the amplifier appears at both outputs and does not therefore contribute any zero error to the reading.

3.7 **Floating Power Supply**

3.7.1 Three supplies are generated:

(a) +5V supply. This is derived from the integrated circuit regulator IC2 which is supplied from the bridge rectifier D3 and reservoir capacitor C3.

(b) +18V supply. This is derived from the integrated circuit regulator IC3. This is a 12V regulator increased to 18V by the series Zener diode D(Z)5. The regulator is supplied from the bridge rectifier D4 and reservoir capacitor C5.

(c) −18V supply. This is generated by the integrated circuit regulator IC4 with series Zener diode D(Z)7. As IC4 is a positive regulator, it is in the 0V line. The regulator is supplied from the bridge rectifier D6 and reservoir capacitor C7.

SECTION 5

MAINTENANCE

1. INTRODUCTION

1.1. This section contains maintenance calibration and service information. Included is a table of recommended test equipment and an in-cabinet performance check that can be used to verify the correct operation of the system.

2. PREVENTIVE MAINTENANCE

WARNING

115V/230V a.c. supply wires are exposed when the top cover is removed. Disconnect the power lead before exposing the internals.

2.1 Cleaning

2.1.1. The unit should be cleaned as often as operating conditions require. Accumulation of dust in the unit can cause overheating and component breakdown. Dust on components acts as an insulating layer thus preventing efficient heat dissipation.

2.1.2. Thoroughly clean the inside and outside of the instrument. Remove the dust from inaccessible areas with low pressure, compressed air. Use alcohol applied with a brush to remove accumulations of dust or grease from connector contacts and component terminals. Clean the exterior of the instrument and the front panel with a mild detergent mixed with water, applying the solution with a soft, lint-free cloth.

2.2. Visual Inspection

2.2.1. The SM 214 should be inspected occasionally for broken connections, loose, broken or frayed wiring, dirty or pitted switch and connector contacts and cracked or broken printed circuit boards. Often, before a failure occurs, a deteriorating component can be located due to obvious discolouration, cracking or warping.

2.2.2. Care must be taken when heat-damaged parts are located. Overheating is usually only a symptom of trouble. For this reason, it is essential to determine the actual cause of overheating before the heat-damaged part is renewed, otherwise, the damage may be repeated.

3. TEST PROCEDURE (ALL VERSIONS)

The following procedure is applicable to all versions of the SM 214 instrument. However, instruments fitted with options SM 260, SM 261 and SM 262 require additional tests; these are detailed in Sub-section 4.

3.1. Test Equipment Required

Item	Description
1	Avometer Model 8 or equivalent
2	Oscilloscope (S.E. Laboratories SM 112 or equivalent)
3	Precision Voltage Source (Fluke type 343A or equivalent)
4	Variac, 0 to 230V.
5	AC Calibrator (Hewlett Packard 745A AC Calibrator and

Test Equipment Required (cont'd)

Item	Description
	746A Amplifier or equivalent) capable of generating 1000V r.m.s. output at 20 kHz)
6	Timer Counter (S.E. Laboratories SM 200 Mk 2 or equivalent).

3.2. Preliminary Steps

(a) Remove the top cover.

(b) Remove the top extrusion.

(c) Remove the floating box cover.

3.3. Power Supplies Check

(a) Unplug the input amplifier board and floating logic boards 1 and 2.

(b) Set the variac (item 4) to 230V r.m.s. Check that the voltage between SKT AB and the negative side of capacitor C1 on the power supply chassis is +5.0V, ±0.2V.

(c) Check that the numerical indicator tubes are illuminated.

(d) Using the negative side of capacitor C5 on the mother board as the 0V reference, check the isolated power supplies on the mother board as detailed in the table below:

Avo Range	Board Pin	Supply Voltage
10V d.c.	at	+5.0V, ±0.2V
25V d.c.	ap	+18.0V, ± 0.8V
25V d.c.	aq	−18.0V, ± 0.8V

(e) Plug-in the three p.c. boards removed in step (a) above. Set the variac to 195V r.m.s., using the Avometer to check the voltage.

(f) Using the test oscilloscope (item 2), referenced to the SM 214 I/P Lo terminal, check the ripple on the +18V, −18V and +5V supplies at the test points shown in the table below.

Supply	Test Point	Location	Ripple (p.p.)
+18V	pin 7	input amplifier board	<150 mV
−18V	pin 12	input amplifier board	<150 mV
+5V (see NOTE)	pin 5	a.c. attenuator board	<150 mV

NOTE To measure the +5V supply ripple, the SM 214 should be set to the 1.1 kV AC range.

(g) With the oscilloscope referenced to the negative side of capacitor C1 on the power supply chassis, check that the ripple on the earthy +5V supply at PL AB is less than 150 mV p.p.

3.4 Functional Check

(a) Unplug SKTAD, SKTAE and SKTAF on display and logic board. Switch on.

(b) Using SM200 Timer Counter set to Range 2, check that clock frequency at IC2 pin 9 display and logic board is 1.2400MHz ±0.0010MHz.

(c) Switch SM 214 off and then on. Check that frequency has not changed.

(d) Select 11V DC range. SM 214 should read −10.9999.

(e) Plug-in all sockets on the display and logic board. Apply voltage inputs to the SM 214 from the precision voltage source in the order detailed in the table below and check that the SM 214 displays the appropriate readings.

Applied Precision Voltage	SM 214 Display Reading (V)
+10.0000V	+10.0000, ± 0.2000
−10.0000V (reverse input leads)	−10.0000, ± 0.2000
0.0000V	±00.0000, ± 0.0010
+ 12.0000V	+ 10.9999
−12.0000V (reverse input leads)	−10.9999
0.0000V	Check that the a.c. sign is illuminated on the a.c. voltage ranges.

(f) Select each range in turn and check that decimal points are illuminated as shown below:

	Range	Tube (numbered from left to right, omitting polarity tube)
DC	110mV	4
	1.1V	2
	11V	3
	110V	4
	1.1kV	5
AC	1.1kV	5
	110V	4
	11V	3
	1.1V	2

(g) Select the 11V DC range. Apply the input voltages in the table below, in the voltage steps shown and check at each voltage point that the correct digit is displayed in the most significant tube of each decade.

Decade	Input Voltages			In Voltage Steps of:
1	+ 1.0000V	to	+9.0000V	1V
2	+0.1000V	to	+0.9000V	0.1V
3	+0.0100V	to	+0.0900V	0.01V
4	+0.0010V	to	+0.0090V	0.001V
5	+0.0001V	to	+0.0009V	0.0001V

(h) Apply +10.0000V from the precision voltage source and depress the SM 214 HOLD push-button. Reduce the voltage source input to +5.0000V and check that the SM 214 reading does not change.

(j) Operate the TRIP push-button. Check that the SM 214 reading changes to +5.0000V, ± 0.1000.

3.5. **Zero Setting Procedure** Repeat 3.5.(a) – (h) for improved ZERO.

(a) Select 11V D.C. range and set both front panel offset controls to mid-position.

(b) Apply a positive voltage from the precision voltage source and adjust this for a reading flickering between +00.0002 and +00.0003. Note this reading as V1.

(c) Repeat step (b), but for a negative voltage input. Note this reading as V2.

(d) Apply a voltage of + $\frac{V1 + V2}{2}$. Adjust RV3, (input amplifier board), for a reading flickering between +00.0002 and +00.0003.

(e) Apply a voltage of +00.00025V. Adjust RV6, floating logic board No.2 for a reading flickering between +00.0002 and +00.0003.

(f) Link the input Hi and input Lo terminals on the SM 214. The SM 214 should read ±00.0000

(g) Adjust RV7, floating logic board No.2 for polarity sign flashing between positive and negative.

(h) Select 1.1V D.C. range and adjust 1.1V front panel offset control for polarity sign flashing between positive and negative and reading of ±0.00000.

3.6. **Input Impedance Check**

(a) Select 11V D.C. range and apply +10.0000V from the precision voltage source. Note the reading.

(b) Connect a 10MΩ resistor in series with the input Hi lead. The change in reading should be less than –0.0100.

3.7. **Input Current Check**

(a) Apply 0.00000V from the precision voltage source, leaving the 10MΩ resistor connected.

(b) Select 1.1V D.C. range. The reading on the SM 214 should be less than ±0.00050.

3.8. **DC Common Mode Rejection Check**

(a) On the SM 214, link the INPUT Lo Terminal to the GUARD terminal and select the 1.1V d.c. range. Connect a resistor, 100kΩ ±5%, between I/P Hi and I/P Lo.

(b) Apply +100.000V to the I/P Hi terminal from the precision voltage source, with the negative terminal of the voltage source grounded. Check that the SM 214 reading is less than +0.00100.

3.9. **AC Common Mode Rejection Check**

(a) On the SM 214 connect the INPUT Lo terminal to the GUARD terminal and select the 1.1V DC range. Connect a resistor, 100kΩ ±5% between I/P Hi and I/P Lo.

(b) Apply 100.00V r.m.s. at 50.25 Hz to the SM 214 from the test a.c. calibrator (item 5) the output high side connected to the I/P Hi terminal of the SM 214. The output low side should be grounded. Check that the SM 214 display reads less than ± 0.00100.

NOTE: Monitor the period of the calibrator output during the test, using the timer counter. The period should be 19.90 ms, ± 0.01 ms.

3.10. Calibration Procedure

(a) Remove the top cover, top extrusion and floating box cover from the SM 214.

(b) On the SM 214, select the 11V DC range, short-out the I/P terminals and switch on. Check that the display reads ±00.0000, ±0.0000. If not, adjust RV3 on the input amplifier board.

(c) Remove the shorting link from the SM 214 INPUT terminals and apply a positive voltage from the precision voltage source (item 3) ; this should be adjusted until the reading on the SM 214 flickers between +00.0002V and +00.0003V. Check that the input voltage on the precision voltage source is between +00.00022V and +00.00028V. If not, carry out the zero setting procedure for the SM 214 as detailed in Para 3.5.

(d) Short-out the SM 214, INPUT terminals and select the 1.1V DC range. Adjust the front panel 1.1V DC OFFSET control until the polarity display on the SM 214 flashes between positive and negative and the display reads ±0.00000, ±0.00000.

(e) Using the table below, set the SM 214 to the ranges listed, apply the appropriate input voltages from the precision voltage source, and adjust the relevant potentiometers to obtain the displayed readings.

Selected SM214 Range	Applied Voltage from Precision Voltage Source (d.c.)	Adjust	Displayed Reading
11V DC	+ 10.0000V	RV11 (floating logic board No. 1)	+10.0000, ±0.0000
11V DC	−10.0000V	RV9 (floating logic board No. 1)	−10.0000, ± 0.0000
1.1V DC	−1.00000V	RV4 (input amplifier board)	−1.00000, ± 0.00000
1.1V DC	+ 1.00000V	—	+1.00000, ±0.00000
1.1kV DC	+ 1000.00V	RV1 (filter board)	+1000.00, ±0.00

(f) Set the precision voltage source to 0V, reverse the input leads to the SM 214, and set the voltage input to −1000.00V. Check that the SM 214 reads −1000.00, ± 0.02.

(g) Set the precision voltage source to −100.000V and select the 110V d.c. range on the SM 214. Check that a reading of −100.000, ± 0.003 is displayed.

(h) Set the precision voltage source to 0V. Reverse the input leads and set the voltage input to +100.000V. Check that the SM 214 display reads +100.000, ± 0.002.

(j) Apply +10.0000V from the precision voltage source, with a 10MΩ , ±5%, resistor connected in series with the I/P Hi lead. Select the 11V DC range on the SM 214. Check that the SM 214 display reads +9.9900V.

(k) Set the precision voltage source to 0V, and select the 1.1V DC range. With the 10MΩ resistor connected as above, check that the SM 214 display reads ± 0.00050.

(m) Select the 11V DC range and disconnect the 10MΩ resistor. Apply +1.0000V, +2.0000V, up to +10.0000V in 1V steps. Check that the reading at each voltage step has an error not greater than ± 0.0002.

3.11. Zener Reference Current Setting Procedure

If any one of the Zener reference diodes (D(Z)20, D(Z)21, D(Z)22 or D(Z)23) is renewed, the instrument must be subjected to a soak test and temperature coefficient check, followed by a current

setting procedure. It is recommended that the instrument be returned to the factory for these procedures.

4. ADDITIONAL TEST PROCEDURES FOR OTHER VERSIONS

All versions of the SM 214 should be subjected to the procedures given for the basic SM 214 version as stated in Sub- section 3. Additional tests must also be applied on those instruments fitted with options. These are given in the table below.

Instrument Version	Option Fitted	Additional Test
SM 214A	SM 260	Refer to Para. 4.2
SM 214B	SM 261	Refer to Para. 4.3
SM 214E	SM 262	Refer to Para. 4.4
SM 214 AB	SM 260, SM 261	Refer to Paras. 4.2 and 4.3
SM 214 AE	SM 260, SM 262	Refer to Paras. 4.2 and 4.4
SM 214 BE	SM 261, SM 262	Refer to Paras. 4.3 and 4.4
SM 214 ABE	SM 260, SM 261, SM 262	Refer to Paras. 4.2, 4.3 and 4.4

4.1 Test Equipment Required

Item	Test Equipment
1	Oscilloscope (S.E. Laboratories SM 112 or equivalent)
2	Precision Voltage Source (Fluke type 342A or equivalent)
3	AC Calibrator (Hewlett Packard 745A AC Calibrator and 746A Amplifier or equivalent)
4	BCD Printer (Sedelec SM 250 or equivalent)
5	SM 214 Printer Cableform

4.2. Setting-up the AC Boards — Option SM 260 (SM 214A, AB, AE and ABE Versions)

If the a.c. convertor board or a.c. attentuator board, or any component on these boards has been renewed, the boards should be re-aligned together as detailed in the following steps.

(a) On the a.c. attenuator board, set the variable capacitors C1, C3 and C5 to mid-position. Set potentiometers RV1, RV2 and RV3 to mid-position

(b) Link all three input terminals on the SM 214

(c) Set RV1 and RV2 on the a.c. convertor board to mid-position

(d) Switch-on the SM 214, select the 1.1V AC range and adjust RV2 on the a.c. convertor board for a reading of 0.00000, $\pm$ 0.00001.

(e) Select the ranges on the SM 214 as detailed in the table below, apply the inputs specified and adjust the appropriate potentiometers for the correct SM 214 readings. The steps in the table should be carried out in the order given.

Step	SM 214 Range	AC Calibrator O/P	Adjust	P.C. Board	For SM 214 Reading
1	1.1V AC	1V r.m.s. at 400Hz	RV1	a.c. convertor	1.00000, ± 0.00005
2		1V r.m.s. at 10 kHz	check	—	1.00000, ± 0.00010
3		0.5000V r.m.s. at 10kHz	check	—	0.50000, ± 0.00005
4	11V AC	10.0000V r.m.s. at 400 Hz	RV3	a.c. attenuator	10.0000, ± 0.0005
5	110V AC	100.000V r.m.s. at 400 Hz	RV2	a.c. attenuator	100.000, ± 0.005
6	1.1 kV AC	600.00V r.m.s. at 400 Hz	RV1	a.c. attenuator	600.00, ± 0.05
7	11V AC	10.0000V r.m.s. at 10 kHz	C5	a.c. attenuator	10.0000, ± 0.0005
8		10.0000V r.m.s. at 5 kHz	check	—	10.0000, ± 0.0010
9	110V AC	100.000V r.m.s. at 10 kHz	C3	a.c. attenuator	100.000, ± 0.005
10		100.000V r.m.s. at 5 kHz	Check	—	100.000, ± 0.010
11	1.1 kV AC	600.00V r.m.s. at 20 kHz	C1	a.c. attenuator	600.00, ± 0.05
12		600.00V r.m.s. at 5 kHz	check	—	600.00, ± 0.10

4.3 **Checking the BCD Outputs Unit — Option SM 261 (SM 214B, AB, BE and ABE Versions)**

(a) Connect the BCD printer (item 4) to the BCD output socket on the rear panel of the SM 214 using the printer cableform (item 5). Switch-on both instruments.

(b) Select the 11V DC range (range 2) and apply +10.0010V from the precision voltage source (item 2).

(c) Depress the HOLD push-button and operate the TRIP push-button. Check that the printer prints out 2 + 100010, ± 5; the 2 denotes range 2 (11V d.c.)

(d) Repeat step (c) above, with range 2 selected, but with each one of the 20 voltages applied in turn. Check that the last six digits of the printed output agrees with the SM 214 display.

+ 8.0000V	+ 4.0000V	+ 2.0000V	+ 1.0000V
+ 0.8000V	+ 0.4000V	+ 0.2000V	+ 0.1000V
+ 0.0800V	+ 0.0400V	+ 0.0200V	+ 0.0100V
+ 0.0080V	+ 0.0040V	+ 0.0020V	+ 0.0010V
+ 0.0008V	+ 0.0004V	+ 0.0002V	+ 0.0001V

(e) Apply −10.0010V, operate the TRIP push-button and check that the printed output is 2−100010, ± 5.

(f) Apply 0.0000V from the precision voltage source. Select each range, in turn, on the SM 214 and check that the printer prints the correct range digit as listed in the table below.

	SM 214 Range	Printed Range Digit
DC	110 mV	0
	1.1V	1
	110V	3
	1.1kV	4
AC	1.1kV	5
	110V	6
	11V	7
	1.1V	8

(g) Disconnect the BCD printer. Apply + 10.0000V from the precision voltage source. Check that the SM 214 can be made to 'trip' by linking pin A8 to pin B8 (0V) on the BCD output connector.

(h) Select the 11V DC range, and apply +10.0000V. Connect the oscilloscope (item 1) so that one beam monitors test point TP 5 on floating logic board No. 2 and the other monitors on pin D6 (end-of-ramp up signal) of the BCD output socket. Check that, with the HOLD push-button released, the signal on pin D6 goes high, coincident with the end of ramp-up, as displayed at TP5.

4.4 Setting-up the 1μV Amplifier Board - Option SM 262 (SM 214E, AE, BE and ABE Versions)

(a) Link together all three INPUT terminals and switch-on the SM 214.

(b) Set RV1 and RV2 on the 1μV amplifier board to mid-position. Set the front panel 110mV DC OFFSET control to mid-position.

(c) Select the 100mV range. Check that the SM 214 display reads ± 000.000, ± 0.025. Note this reading as V1.

(d) Replace the link between the INPUT Hi and INPUT Lo terminals with a resistor, 10MΩ ± 5%. Adjust RV2 on the 1μV amplifier board for a displayed reading of V1, ± 0.400.

(e) Short-out the INPUT terminals (remove 10MΩ resistor). Set the front panel 110mV DC OFFSET control for a reading of ± 000.000, ± 0.001.

(f) Apply 0.000 mV as set-up on the precision voltage source to the SM 214 and note any zero offset reading on the SM 214.

(g) Change the precision voltage source output to +100.000 mV. Adjust potentiometer RV1 on the 1μV amplifier board for a reading of +100.000, ± 0.002, allowing for the zero offset value noted in (f) above.

(h) Change the precision voltage output to +50.000 mV. Check that the SM 214 reads + 50.000, ± 0.003, allowing for the zero offset value noted in (f) above.

(j) Reverse the INPUT leads at the precision voltage source output terminals and apply 0.000 mV to the SM 214. Note any zero offset reading on the SM 214.

(k) Change the precision voltage source output to −100.000 mV. Check that the SM 214 reads −100.000, ± 0.003 allowing for the zero offset value noted in (j) above.

(m) Change the precision voltage source output to −50.000 mV. Check that the SM 214 reads −50.000, ± 0.003, allowing for the zero offset value noted in (j) above.

5. RENEWAL OF INDICATOR TUBES V1 to V7

The procedure used to renew an indicator tube is detailed in fig. 3, at the back of this manual.

SECTION 6

COMPONENT LISTS

1. INTRODUCTION

1.1. This section contains information for ordering replaceable parts. Tables 6.1 to 6.13 provide the following information:-

(a) Circuit reference (where applicable)

(b) Manufacturer/reference

(c) S.E.L. Part No.

(d) Value, tolerance and rating of component (where applicable).

1.2. Minor items, such as screws, nuts, etc., have not been included as they are not considered special to the equipment.

2, ORDERING INFORMATION

2.1. To order your replacement part address the order to your local agent or to *Service Department, S.E. Laboratories (Engineering) Ltd., North Feltham Trading Estate, Feltham, Middlesex. Tel. No: 01-890-1166 or Northern Sales Office, Tel. No: Sandiacre 3255.*

2.2. Specify the following information for each part:-

(a) Model and serial number of the equipment.

(b) S.E.L. part number.

(c) Circuit reference

(d) Description and Manufacturer's reference.

TABLE 6.1 **INPUT ATTENUATOR FILTER BOARD (FIG 1)** **PL 31633**

Cct. Ref.	S.E.L. Part No.	Manufacturer/Reference	Value	Tol ± %	Rating
		Resistors (fixed) Ω			
R3 R4 R5 R6 R7	DS 32834	Matched set:- R3 thru R5:- Mann components, 3F. R6: Mann components, 3F. R7: Mann components, 3C.	 2.5M 2.4M 99.950k		
		Resistor (variable) Ω			
RV1	FS 10462	Greenwood, ET 12L	100		

TABLE 6.2 **INPUT AMPLIFIER BOARD (FIG 1)** PL 33953

Cct. Ref.	S.E.L. Part No.	Manufacturer/Reference	Value	Tol ± %	Rating
		Capacitor (μF)			
C1	CS 4779	Suflex, HS 2200/20-15/100	2200p	10	160V
C2	CS 30886	Suflex, HS 2/10-28/63	0.2	10	63V
C3	CS 30088	Suflex, HS 100/10-7/160	100p	10	160V
C4	CS 4684	Wyma, MKS	2.2	20	63V
C4a	As C4				
C5	CS 31336	Suflex, HS 390/10-7/160	390p	10	160V
		Diodes			
D1 thru' D7	BS 2045	Mullard, 1N 914			
		Resistors (fixed) Ω			
R1					
R2					
R3					
R4					
R5					
R6	DS 33943	Mullard, CR25	470	5	¼W
R7	DS 33947	Mullard, CR25	2.2k	5	¼W
R8	DS 33836	Mullard, CR25	100k	5	¼W
R9	DS 33951	Mullard, CR25	15k	5	¼W
R10					
R11	DS 33996	Mullard, CR25	10	5	¼W
R12	DS 33954	Mullard, CR25	22k	5	¼W
R13	DS 33993	Mullard, CR25	3.3k	5	¼W
R14	DS 34040	Mullard, CR25	47k	5	¼W
R15	DS 33951	Mullard, CR25	10k	5	¼W
R16	As R13				
R17		Selected on test from the following:			
	DS 34039	Mullard, CR25	39k	5	¼W
	DS 33955	Mullard, CR25	33k	5	¼W
	DS 34037	Mullard, CR25	27k	5	¼W
	DS 33954	Mullard, CR25	22k	5	¼W
	DS 34035	Mullard, CR25	18k	5	¼W
	DS 33953	Mullard, CR25	15k	5	¼W
R18	As R8				
R19	As R12				
R20	As R13				
R21	DS 34037	Mullard, CR25	27k	5	¼W
R22	DS 34004	Mullard, CR25	47	5	¼W
R23	As R14				
R24	DS 34053	Mullard, CR25	560k	10	¼W
R25	As R8				
R26	As R14				
R27	As R14				

TABLE 6.2 (cont'd)

Cct. Ref.	S.E.L. Part No.	Manufacturer/Reference	Value	Tol ± %	Rating
R28	DS 32801	Mann Components	20k		
R29			2.221k		
R30	As R7				
R31	DS 33949	Mullard, CR25	4.7	5	¼W
R32	As R21				
R33	DS 34327	Welwyn, 4032G	1	1	1/16W
		Resistors (variable) Ω			
RV3	FS 10461	Greenwood, ET 43P	1k		
RV4	As RV3				
		Transistors and Integrated Circuits			
TR1	BS 2519	Mullard, BCY 72			
TR2	BS 2537	Mullard, BC 107			
TR3	As TR2				
TR4	BS 2644	Siliconix, 2N 4119			
TR5	As TR4				
TR6	As TR4				
TR7	As TR2				
TR8	As TR4				
TR9	As TR1				
TR10	BS 2976	Siliconix, E 112A			
TR11	As TR1				
TR12	BS 3157	Siliconix, E 112			
OA1	BS 3109	Computing Techniques, S 140			
		Miscellaneous			
ILP1	JS 14080	Neon, Hivac 34L			
	BS 2228	Transistor mounting pad, Jermyn TO 18-001. (All TR's except 4 and 5)			

TABLE 6.3 **FLOATING LOGIC BOARD No. 1 (FIG 1)** **PL 33974**

Cct. Ref.	S.E.L. Part No.	Manufacturer/Reference	Value	Tol ± %	Rating
		Capacitors (μF)			
C13	CS 4185	Suflex, HS 1000/2½-10/30	1000p	2.5	30V
C14	As C13				
C15	CS 31120	Erie, 831/T/25	0.01	+50, -25	25V
C16	As C15				
C17	As C15				
C18	CS 4610	Suflex, HS 470/20 - 7/160	470p	20	160V
C19	As C15				
C20	As C15				
		Diodes			
D24, D25	BS 2045	Mullard, 1N 914			
		Resistors (fixed) Ω			
R62	DS 33943	Mullard, CR25	470	5	¼W
R63	As R62				
R64	DS 33531	Mullard, CR25	619	5	¼W
R65	DS 34336	Morganite, FC65	1.37k	1	
R66	DS 34335	Morganite, FC65	4.22k	5	
R67	DS 33940	Mullard, CR25	120	5	¼W
R68	—	Selected-on-test (see list at end of resistor table)			
R69	DS 33949	Mullard, CR25	4.7k	5	¼W
R70	DS 34048	Mullard, CR25	220k	5	¼W
R71	DS 34040	Mullard, CR25	47k	5	¼W
R72	As R71				
R73	As R69				
R74	As R70				
R75	—	Selected-on-test (see list at end of resistor table)			
R76	As R67				
R77	As R65				
R78	As R66				
R79	As R64				
R80	DS 33996	Mullard, CR25	10	5	¼W
R81	As R80				
R82	DS 34022	Mullard, CR25	1.5k	5	¼W
R83	DS 34023	Mullard, CR25	1.8k	5	¼W
R84	As R82				
R85	As R82				
R86	As R83				
R87	As R82				
R88	DS 34013	Mullard, CR25	270	5	¼W
R89	As R82				
R90	As R82				
R91	As R82				
R92	As R82				

TABLE 6.3 (cont'd)

Cct. Ref.	S.E.L. Part No.	Manufacturer/Reference	Value	Tol ± %	Rating
R93	As R82				
R94	DS 33947	Mullard, CR25	2.2k	5	¼W
R95	As R82				
R96	As R82				
		Selected-on-test values for R68 and R75:–			
	DS 34337	Morganite, FC65	665	1	
	DS 34338	Morganite, FC65	634	1	
	DS 32987	Morganite, FC65	604	1	
	DS 34340	Morganite, FC65	576	1	
	DS 34341	Morganite, FC65	549	1	
	DS 34342	Morganite, FC65	523	1	
	DS 34343	Morganite, FC65	487	1	
	DS 34344	Morganite, FC65	453	1	
		Resistors (variable) Ω			
RV9	FS 10459	Greenwood, ET 34P	200		
RV10	FS 10468	Greenwood, ET 34P	2k		
RV11	As RV9				
		Transistors and Integrated Circuits			
TR18	BS 2519	Mullard, BCY 72			
TR19	As TR18				
TR20	BS 2976	Siliconix, E 112A			
TR21	BS 2537	Mullard, BC 107			
TR22	BS 3157	Siliconix, E 112			
TR23	As TR21				
TR24, TR25, TR26, TR27, TR28	BS 2599	Mullard, BS X 20			
IC2, IC3	BS 2929	Texas, SN 72741L			
IC4, IC5	BS 7473	Texas, SN 7473N			
IC6, IC7	BS 7400	Texas, SN 7400N			
IC8	BS 7410	Texas, SN 7410N			

Cct. Ref.	S.E.L. Part No.	Manufacturer/Reference	Value	Tol ± %	Rating
		Capacitors (μF)			
C6	CS 30727	Wima, MKS	0.68	20	100V
C7	CS 30343	Erie, 831/T/30	0.1	+50, −25	30V
C8	CS 31340	Wima, 602.4	0.39	10	63V
C9	As C7				
C10	As C7				
C11	CS 31338	Suflex	0.03	10	63V
C12	CS 30629	Suflex, HS 2200/2½-7/30	2200p	2.5	30V
		Diodes			
D8, D9	BS 2069	Mullard, OA 200			
D10 thru' D15	BS 2045	Mullard, 1N 914			
D(Z)16	BS 2689	Mullard, BZY 88 C12			
D17, D18	BS 2045	Mullard, 1N914			
D(Z)19	BS 3101	Mullard, BZY 88 C6V2			
		Resistors (fixed) Ω			
R34, R35		Selected-on-test from:			
	DS 34432	Morganite, FC65	5.4k	1	
	DS 34333	Morganite, FC65	3.6k	1	
	DS 34334	Morganite, FC65	1.8k	1	
R36	DS 33993	Mullard, CR25	3.3k	5	¼W
R37	DS 33943	Mullard, CR25	470	5	¼W
R38	DS 34040	Mullard, CR25	47k	5	¼W
R39	DS 34330	Morganite, FC65, 15ppm	499k	1	
R40	DS 33951	Mullard, CR25	10	5	¼W
R41	DS 33837	Mullard, CR25	100	5	¼W
R42	As R37				
R43	As R41				
R44	As R41				
R45	DS 34029	Mullard, CR25	5.6k	5	¼W
R46	DS 33836	Mullard, CR25	100k	5	¼W
R47	As R45				
R48	DS 34037	Mullard, CR25	27k	5	¼W
R49	DS 34013	Mullard, CR25	270	5	¼W
R50	DS 33954	Mullard, CR25	22k	5	¼W
R51	As R36				
R52, R53	DS 33953	Mullard, CR25	15k	5	¼W

TABLE 6.4 (cont'd)

Cct. Ref.	S.E.L. Part No.	Manufacturer/Reference	Value	Tol ± %	Rating
R54	DS 33945	Mullard, CR25	1k	5	¼W
R55	As R37				
R56	DS 34057	Mullard, CR25	4.7M	10	¼W
R57	As R54				
R58	As R46				
R59	DS 33965	Mullard, CR25	2.2M	5	¼W
R60	As R37				
		Resistors (variable) Ω			
RV5	FS 10468	Greenwood, ET 34P	2k		
RV6	FS 10467	Greenwood, ET 34P	10k		
RV7	FS 10297	Plessey, 404/8/0285/MPD/PC, LIN.	470		¼W
		Transistors and Integrated Circuits			
TR13	BS 2976	Siliconix, E 112A			
TR14	BS 2519	Mullard, BCY 72			
TR15	BS 2537	Mullard, BC 107			
TR16	As TR14				
TR17	As TR15				
IC1	BS 2650	Texas, SN 72710L			
OA1	BS 3103	Computing Techniques S141			
		Miscellaneous			
—	BS 2751	Transistor Mounting Pad, Milton Ross, 10277 (IC1)			
—	BS 2228	Transistor Mounting Pad, Jermyn TO-18-001 (TR13 to TR17 incl.)			

TABLE 6.5 **FLOATING BOX COMPONENTS (FIG 1)** **PL 33871**

Cct. Ref.	S.E.L. Part No.	Manufacturer/Reference	Value	Tol ± %	Rating
		Resistors (fixed) Ω			
R1	DS 33836	Mullard, CR25	100k	5	¼W
R61	DS 34367	Mullard, CR25	2.7M	10	¼W
		Resistors (variable) Ω			
RV2	FS 10352	Reliance, CW05	10k		
RV8	FS 10421	Reliance, CW05	50k		

TABLE 6.6 **FRONT PANEL COMPONENTS (FIG 1)** **PL 33864**

Cct. Ref.	S.E.L. Part No.	Manufacturer/Reference	Value	Tol ± %	Rating
SW1	QS 22374	Rotary switch, AB Electronic Components (S.E.L. D 33866)			
J/PHi	C 31616	Terminal, red, Lebury & Co. (Metals) Ltd.			
I/PLo	C 31616/02	Terminal, black, Lebury & Co. (Metals) Ltd.			
GUARD	C 31616/01	Terminal, green, Lebury & Co. (Metals) Ltd.			

NOTE: HOLD and TRIP push-buttons are listed on Table 6.10
DC OFFSET controls (RV2 and RV8) are listed on Table 6.5

TABLE 6.7 **FLOATING POWER SUPPLY BOARD (FIG 5)** **PL 33984**

Cct. Ref.	S.E.L. Part No.	Manufacturer/Reference	Value	Tol ± %	Rating
		Capacitors (μF)			
C3	CS 30500	Mullard, 01715102	1000		16V
C4	CS 30176	Mullard, 01516109	10		25V
C5	CS 31068	Mullard, 01717471	470		40V
C6	As C4				
C7	As C5				
C8, C9, C10	As C4				
		Diodes			
D(Z)5, D(Z)7	BS 2525	Mullard, 6V2			
D(Z)20 thru' D(Z)	BS 2797	Motorola, 1N 829 NOTE: D(Z) 20 & 22, D(Z) 21 & 23 are moulded pairs to spec. D 40440 (BS 3134)	shown on Fig 1		
		Heatsink Assembly PL 33886			
D3, D4, D6	BS 3113	Mullard, OSH01-100			
D(Z)8, D(Z)9	BS 2699	Mullard, BZY 88 C15			
IC2	BS 3055	S.G.S. L005			
IC3, IC4	BS 3056	S.G.S. L036			
T2	ES 8459	Mains Transformer D3089, Parmeko			

TABLE 6.8 **EARTHY POWER SUPPLY (FIG 5)** **PL 33888**

Cct. Ref.	S.E.L. Part No.	Manufacturer/Reference	Value	Tol ± %	Rating
		Capacitor (μF)			
C1	CS 31339	Mullard, 071-15472	4700		16V
C2	CS 30176	Mullard, 01516109	10		25V
		Diodes			
D1	BS 3114	Diodes Ltd, BR 705A			
D2	BS 2522	Mullard, BY X 10			
		Integrated Circuit			
IC1	BS 3115	National Semi-Conductors LM 309K			
		Transformer			
T1	ES 8458	Mains, D3076, Parmeko			

TABLE 6.9 **MOTHER BOARD (FIG 1)** **PL 33976**

Cct. Ref.	S.E.L. Part No.	Manufacturer/Reference	Value	Tol ± %	Rating
		Connectors			
SKTA, SKTC	AS 1594	Female, 4-way, AMP, 163680-2			
SKTB, SKTD	AS 1595	Female, 6-way, AMP, 163680-4			
		Transformers			
T4, T5	ES 8360	Buckingham Electronic Engineering, BE 68130			

Cct. Ref.	S.E.L. Part No.	Manufacturer/Reference	Value	Tol ± %	Rating
		Capacitors (µF)			
C2	CS 4117	Suflex, HS 1500/10.7/30	1500p	10	30V
C3	CS 4048	Suflex, HS 330/10-7/160	330p	10	160V
C4	CS 31120	Erie, 831/T/25V	0.01	+50, −25	25V
C5	As C4				
C6	CS 30166	Mullard, C280AE/P100K	0.1	20	250V
C7 Thru' C23	CS 31120	Erie, 831/T/25V	0.01	+50, −25	25V
C24	CS 30554	Suflex, HS 470/10-7/160	470p	10	160V
C25	CS 31335	Suflex, HS 33/10-7/160	33p	10	160V
C26	CS 30612	Suflex, KSN	100p	10	63V
		Diodes			
D1 D2	DS 2045	Mullard, 1N914			
		Resistors (fixed) Ω			
R1	DS 33954	Mullard, CR25	22k	5	¼W
R2	DS 33951	Mullard, CR25	10k	5	¼W
R3	As R1				
R4 R5 R6	DS 34022	Mullard, CR25	1.5k	5	¼W
R7 R8 R9	DS 33954	Mullard, CR25	22k	5	¼W
R10	DS 33943	Mullard, CR25	470	5	¼W
R11	As R7				
R12	DS 34013	Mullard, CR25	270	5	¼W
R13	As R10				
R14	As R1				
R15 R16	DS 34022	Mullard, CR25.	1.5k	5	¼W
R17	DS 33945	Mullard, CR25	1k	5	¼W
R18	As R15				
R19	DS 33948	Mullard, CR25	2.7k	5	¼W
R20 R21	DS 34023	Mullard, CR25	1.8k	5	¼W
R22 R23 R24 R25	DS 34022	Mullard, CR25	1.5k	5	¼W
R26 R27	DS 33996	Mullard, CR25	10	5	¼W

TABLE 6.10 (cont'd)

Cct. Ref.	S.E.L. Part No.	Manufacturer/Reference	Value	Tol ± %	Rating
R28	As R10				
		Transistors and Integrated Circuits			
TR1	BS 2599	Mullard, BSX 20			
TR2, TR3	BS 2886	Mullard, BSX 21			
TR4, TR5, TR6, TR7	BS 2599	Mullard, BSX 20			
IC1	BS 7413	Texas, SN 7413N			
IC2, IC3	BS 7473	Texas, SN 7473N			
IC4	BS 7400	Texas, SN 7400N			
IC5	BS 7541	Texas, SN 74141N			
IC6	BS 7475	Texas, SN 7475N			
IC7	BS 7490	Texas, SN 7490N			
IC8	BS 7521	Texas, SN 74121N			
IC9	As IC5				
IC10	As IC6				
IC11	As IC7				
IC12	As IC5				
IC13	As IC6				
IC14	As IC7				
IC15	BS 7402	Texas, SN 7402N			
IC16	BS 7420	Texas, SN 7420N			
IC17	As IC2				
IC18	BS 7430	Texas, SN 7430N			
IC19	BS 7400	Texas, SN 7400N			
IC20	As IC5				
IC21	As IC6				
IC22	As IC7				
IC23	As IC2				
IC 24	As IC5				
IC25	As IC6				
IC26	As IC7				
IC27, IC28	As IC2				
IC29	As IC6				
IC30	BS 7410	Texas, SN 7410N			
IC31, IC32	As IC4				
IC33	As IC5				
IC34, IC35	As IC16				

TABLE 6.10 (Cont'd)

Cct. Ref.	S.E.L. Part No.	Manufacturer/Reference	Value	Tol ± %	Rating
		Miscellaneous			
	WS 28851	Crystal, 2.48 MHz, McKnight Crystals, Type MD (Parallel Resonance with 30pF)			
V1 thru' V6	WS 28782	Indicator tube, J.T.T., type 5870-L			
V7	WS 28850	Indicator tube, I.T.T., type 58-GS-S.			
–	KS 15351	Tube spacer, K.G.M.			
SKT AC SKT AD SKT AE SKT AF	AS 1595	Connector, female, 6-way AMP, 163680-4			
–	BS 2228	Transistor mounting pad TO18-001, AEI (TR1 to TR7)			
HOLD TRIP	QS 22375	Push-button, Lipa Isotat			

TABLE 6.11 AC CONVERTER AND ATTENUATOR – OPTION SM 260 (FIG 6) PL

Cct. Ref.	S.E.L. Part No.	Manufacturer/Reference	Value	Tol ± %	Rating
		Attenuator Board			
		Capacitor (fixed)			
C2	CS 31098	Suflex, HS 1000/10-7/160	1000p	10	160
C4	CS 30088	Suflex, HS 100/10-7/160	100p	10	160
C6	CS 30574	Suflex, HS 10/10-7/160	10p	10	160
		Capacitors (variable)			
C1, C3, C5	CS 30814	Jackson Bros., style 408	0.25p to 8pF		
		Resistors (fixed) Ω			
R1	DS 33172	Welwyn, 4337D, 25ppm	1M	0.25	
R2	DS 34325	Morganite, FC65, 25ppm	995	0.25	
R3	DS 33173	Welwyn, 4337D, 25ppm	990k	0.25	
R4	DS 34329	Morganite, FC65, 25ppm	9.95k	0.25	
R5	DS 33174	Welwyn, 4337D, 25ppm	900k	0.25	
R6	DS 34328	Morganite, FC65, 25ppm	99.5k	0.25	
		Resistors (variable) Ω			
RV1	FS 10511	Greenwood ET 34P	10		
RV2	FS 10510	Greenwood ET 34P	1k		
RV3	FS 10461	Greenwood ET 34P	1k		
		Relays			
RL1 thru' RL4	HS 12129	Reed relay, Astralux, GB 821 A-3.			
		AC Converter Board			
		Capacitors (fixed) µF			
C1, C2	CS 30537	Mullard, C280AE/P47k	0.47	20	250V
C3, C4	CS 30088	Suflex, HS 100/10-7/160	100p	10	160V

TABLE 6.11 (cont'd)

Cct. Ref.	S.E.L. Part No.	Manufacturer/Reference	Value	Tol ± %	Rating
C5	CS 30574	Suflex, HS 10/10-7/160	10p	10	160V
C6	CS 30252	Suflex, HS 220/10-7/160	220p	10	160V
C7	CS 30811	Union Carbide, Kemet J	100	20	10V
C8					
C9	CS 30343	Erie, 811/T/30V	0.1	+50, −25	30V
C10					
C11	CS 4684	Waycom, MKS	2.2	20	60V
C12	CS 4684	Waycom, MKS	2.2	20	60V
C13	CS 30602	Waycom, MKS	0.47	20	100V
C14	CS 30606	Waycom, MKS	1.0	20	100V
C15	As C9				
C16	As C14				
		Diodes			
D1, D2	BS 2856	Siliconix, PAD 20			
D3, D4	BS 2045	Mullard, 1N914			
D(Z)5	BS 2806	Transitron, 1N821			
D(Z)6	BS 2682	Mullard, BZY 88 C6V2			
D7, D8	BS 2906	Celdis, MBD 101			
D(Z)9, D(Z)10, D(Z)11, D(Z)12	BS 2627	Mullard, BZY 88 C6V8			
		Resistors (fixed) Ω			
R1	DS 33954	Mullard, CR25	22k	5	¼W
R2, R3	DS 34026	Mullard, CR25	3.3k	5	¼W
R4, R5	DS 34057	Mullard, CR25	4.7M	5	¼W
R6	DS 34022	Mullard, CR25	1.5k	5	¼W
R7	DS 34035	Mullard, CR25	18k	5	¼W
R8	As R6				
R9	DS 34027	Mullard, CR25	3.9k	5	¼W
R10, R11	As R1				
R12	As R9				
R13	As R6				
R14	DS 34006	Mullard, CR25	68	5	¼W

TABLE 6.11 (cont'd)

Cct. Ref.	S.E.L. Part No.	Manufacturer/Reference	Value	Tol ± %	Rating
R15	As R6				
R16	As R7				
R17	As R12				
R18	DS 33959	Mullard, CR25	330k	5	¼W
R19					
R20	DS 34098	Mullard, MR25	47.5k	1	
R21	DS 33152	Morganite, FC65, 25ppm	7.68k	0.25	
R22	DS 34040	Mullard, CR25	47k	5	¼W
R23	As R21				
R24	As R20				
R25	As R22				
R26	DS 34326	Morganite, FC65, 25ppm	11.1k	0.25	
R27	DS 33941	Mullard, CR25	220	5	¼W
R28	DS 33837	Mullard, CR25	100	5	¼W
R29	As R22				
		Resistors (variable) Ω			
RV1	FS 10458	Greenwood, ET 34P	500		
RV2	FS 10510	Greenwood, ET 34P	100		
		Transistors			
TR1, TR2	BS 3044	Dual FET, Siliconix U257			
TR3, TR4	BS 2838	Motorola, MPS 3640			
TR5	BS 2835	R.C.A., 2N 5179			
TR6	BS 2775	Mullard, BCY 70			
TR7	BS 2537	Mullard, BC107			

TABLE 6.12 **BCD OUTPUTS UNIT – OPTION SM 261 (FIG 7)** **PL 33950**

Cct. Ref.	S.E.L. Part No.	Manufacturer/Reference	Value	Tol ± %	Rating
		Capacitors (μF)			
C1, C2	CS 31120	Erie, 831/T/25	0.01	+50, −25	25V
		Diodes			
D(Z)1	BS 2682	Mullard, BZY 88 C6V2			
		Fuse			
FS1	RS 23125	Bulgin, F290/.250A			
		Integrated Circuits			
IC1	BS 7404	Texas SN 7404N			
IC2 thru' IC7	BS 7408	Texas, SN 7408N			
		Connectors			
	AS 1460	Socket, 34-way, McMurdo, MS 134			
	AS 500	Plug, 34-way, McMurdo, MP 134			
	AS 501	Short cover top for plug, McMurdo, MC 134-S			
	AS 0427	Hinge plate (1 pair), McMurdo type ML/H.			
	AS 0426	Locking plate (1 pair), McMurdo, type ML/L			

TABLE 6.13 **1μV AMPLIFIER BOARD – OPTION SM 262 (FIG 8)** PL 33971

Cct. Ref.	S.E.L. Part No.	Manufacturer/Reference	Value	Tol ± %	Rating
		Capacitors (μF)			
C1	CS 30602	Waycom, MKS	0.47	20	100V
C2, C3	CS 30309	Erie, 861/T/18V	0.01		18V
C4	CS 31337	Waycom, MKS	0.47	20	250V
		Diodes			
D1, D2	BS 2856	Siliconix, PAD 20			
		Integrated Circuit			
OA1	BS 2891	Non-inverting chopper amplifier, Analog Devices, 260k			
		Resistors (fixed) Ω			
R1	DS 32801	Matched pair, Mann components	20k		
R3			2.22k		
R2	DS 34327	Welwyn, 4032G	1	1	
R4	DS 33953	Mullard, CR25	15k	5	¼W
R5		Selected-on-test from:-			
	DS 34054	Mullard, CR25	680k	5	¼W
	DS 34051	Mullard, CR25	390k	5	¼W
	DS 34049	Mullard, CR25	270k	5	¼W
	DS 34048	Mullard, CR25	220k	5	¼W
	DS 34047	Mullard, CR25	180k	5	¼W
R6, R7	DS 33942	Mullard, CR25	330	5	¼W
R8	DS 33955	Mullard, CR25	33k	5	¼W
R9	DS 33969	Welwyn, 4032G	2	1	
R10	DS 34054	Mullard, CR25	680k	5	¼W
R11	DS 33965	Mullard, CR25	2.2M	5	¼W
R12	DS 33962	Mullard, CR25	1M	5	¼W
R13	DS 34045	Mullard, CR25	220k	5	¼W
		Resistors (variable) Ω			
RV1	FS 10461	Greenwood, ET 34P	1k		
RV2	FS 10467	Greenwood, ET 34P	10k		

SECTION 7

CIRCUIT AND COMPONENT LAYOUT DIAGRAMS

CIRCUIT DIAGRAM CHANGES

APRIL 1973

FIG.1 FLOATING SECTION - CIRCUIT DIAGRAM – E 33945

Input Amplifier P.C.B.	R24 was 1.2MΩ R24 now 560kΩ
Floating Logic P.C.B. No.2	R56 was 8.2MΩ R56 now 4.7MΩ

FIG.4 MAIN LOGIC AND DISPLAY BOARD – CIRCUIT DIAGRAM E40428/1

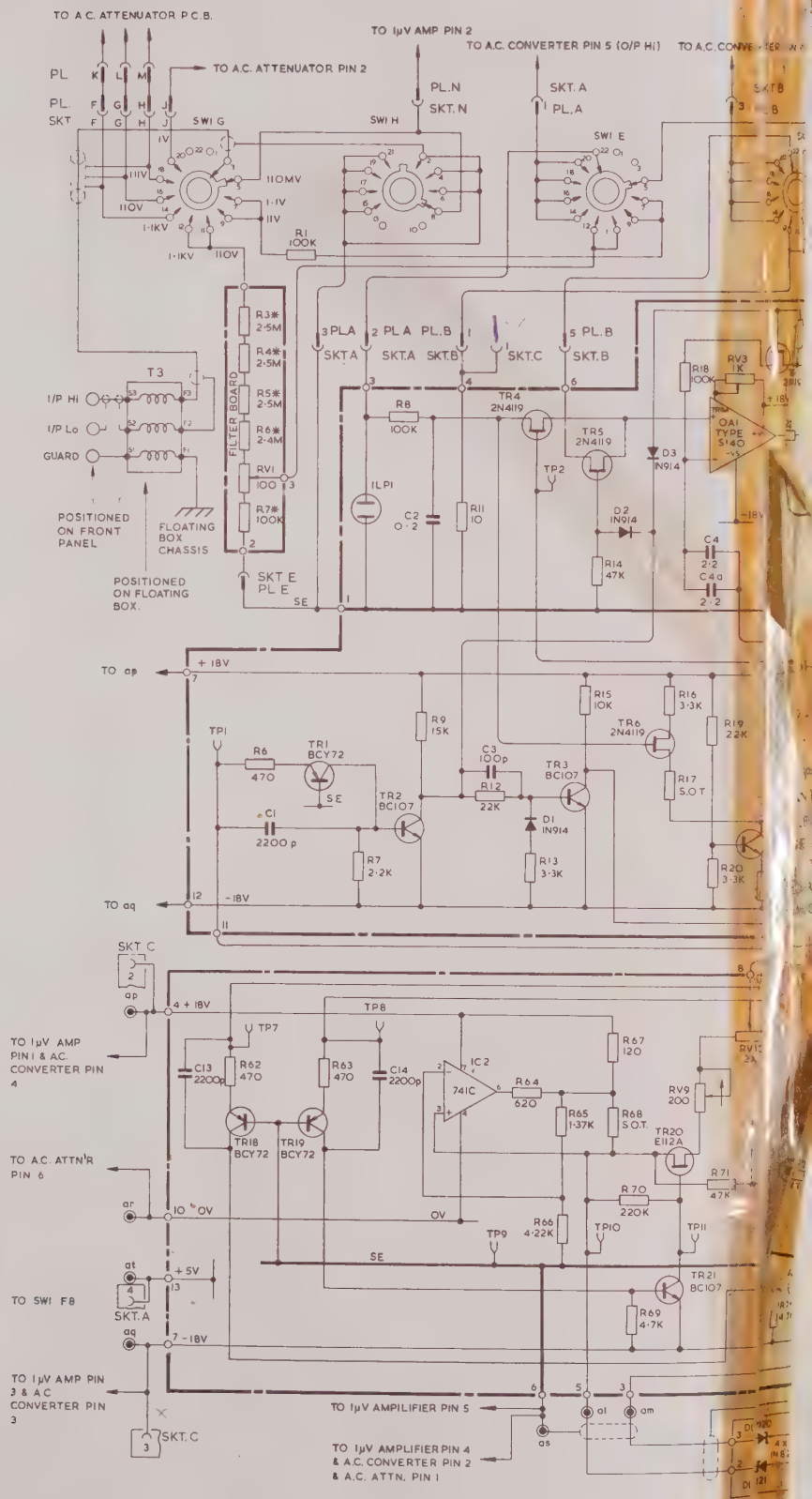
C24 was 220p
C24 now 470p

FIG.5 POWER SUPPLY – CIRCUIT AND COMPONENT LAYOUT

Floating Section Power Supply	Two zener diodes added as follows:- D(Z)8 connected across IC3 input and output pins, cathode (+) to input. D(Z)9 connected across IC4 input and output pins, cathode (+) to input. Diodes are Mullard, BZY 88 C15

FIG.8 1μV AMPLIFIER BOARD (OPTION SM262) – CIRCUIT AND COMPONENT LAYOUT DIAGRAMS

Circuit Diagram D33987/1	R5 was 1MΩ R5 now selected-on-test from 180k, 220k, 270k, 390k, 680k.


TO A.C. ATTENUATOR P.C.B.
TO 1μV AMP PIN 2
TO A.C. CONVERTER PIN 5 (O/P Hi)
TO A.C. ATTENUATOR PIN 2
PL
PL. SKT
SWI G
SWI H
SWI E
PL.N
SKT. N
SKT. A
PL. A
SKT B
R1 100K
R3* 2·5M
R4* 2·5M
R5* 2·5M
R6* 2·4M
RV1 100
R7* 100K
FILTER BOARD
T3
I/P HI
I/P Lo
GUARD
POSITIONED ON FRONT PANEL
FLOATING BOX CHASSIS
POSITIONED ON FLOATING BOX.
SKT E PL E
SE
PL A
PL B
SKT A
SKT B
SKT C
R8 100K
TR4 2N4119
TR5 2N4119
D3 IN914
D2 IN914
R14 47K
C4 2·2
C4a 2·2
RV3 1K
R18 100K
OA1 TYPE S140
+18V
-18V
ILP1
C2 0·2
R11 10
TP2
TO ap
TO aq
+18V
-18V
TP1
R6 470
TR1 BCY72
C1 2200p
R7 2·2K
TR2 BC107
R9 15K
C3 100p
R12 22K
TR3 BC107
D1 IN914
R13 3·3K
R15 10K
TR6 2N4119
R16 3·3K
R17 S.O.T
R19 22K
R20 3·3K
SKT C
ap
aq
ar
at
4 +18V
10 0V
+5V
7 -18V
TP8
TP7
TO 1μV AMP PIN 1 & AC. CONVERTER PIN 4
TO A.C. ATTN'R PIN 6
TO SW1 F8
TO 1μV AMP PIN 3 & A.C CONVERTER PIN 3
C13 2200p
R62 470
R63 470
C14 2200p
TR18 BCY72
TR19 BCY72
IC2 741C
R64 620
R65 1·37K
R67 120
R68 S.O.T.
RV9 200
TR20 E112A
R71 47K
R70 220K
R66 4·22K
TP9
TP10
TP11
0V
SE
TR21 BC107
R69 4·7K
TO 1μV AMPLIFIER PIN 5
TO 1μV AMPLIFIER PIN 4 & A.C. CONVERTER PIN 2 & A.C. ATTN. PIN 1
al
am
as

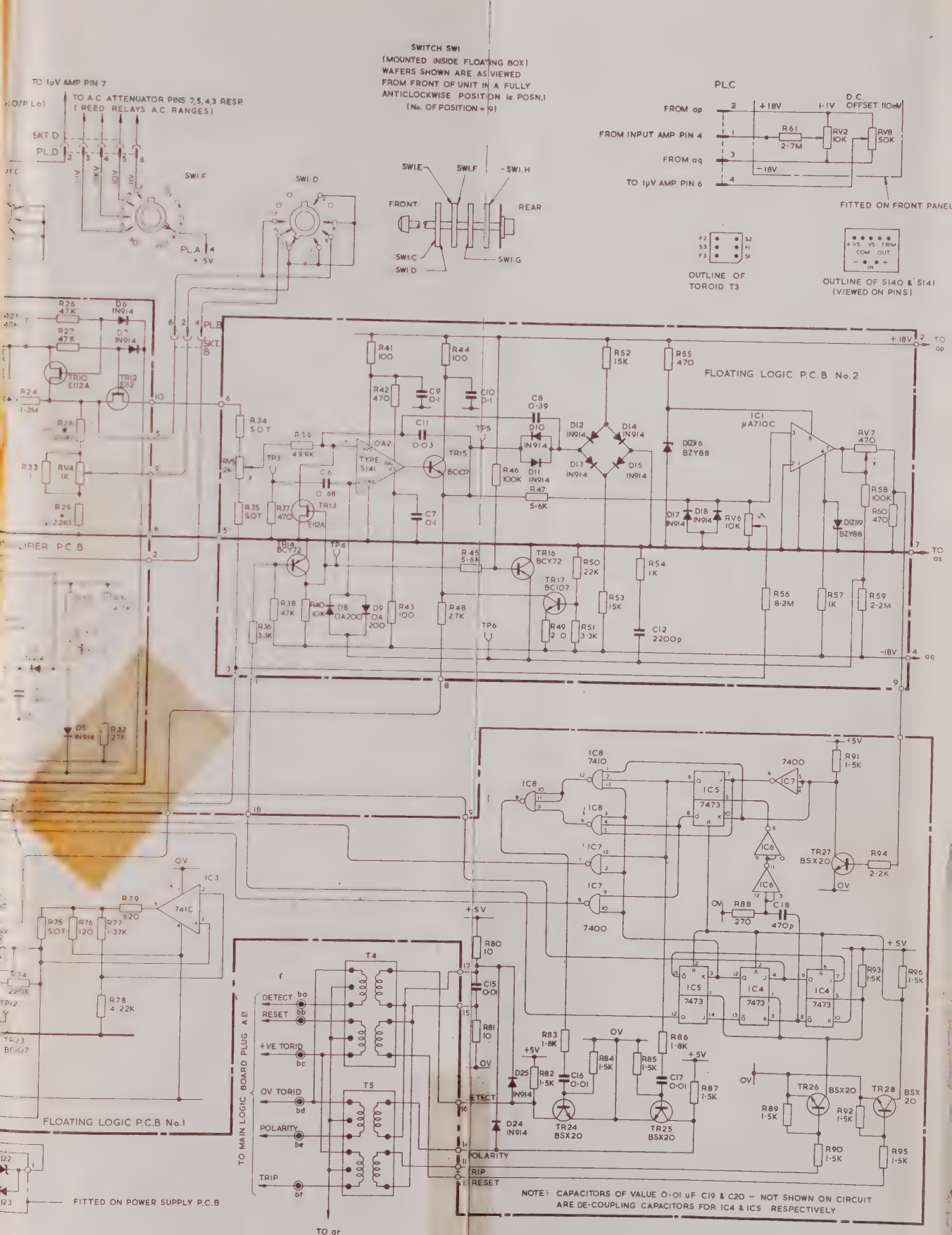
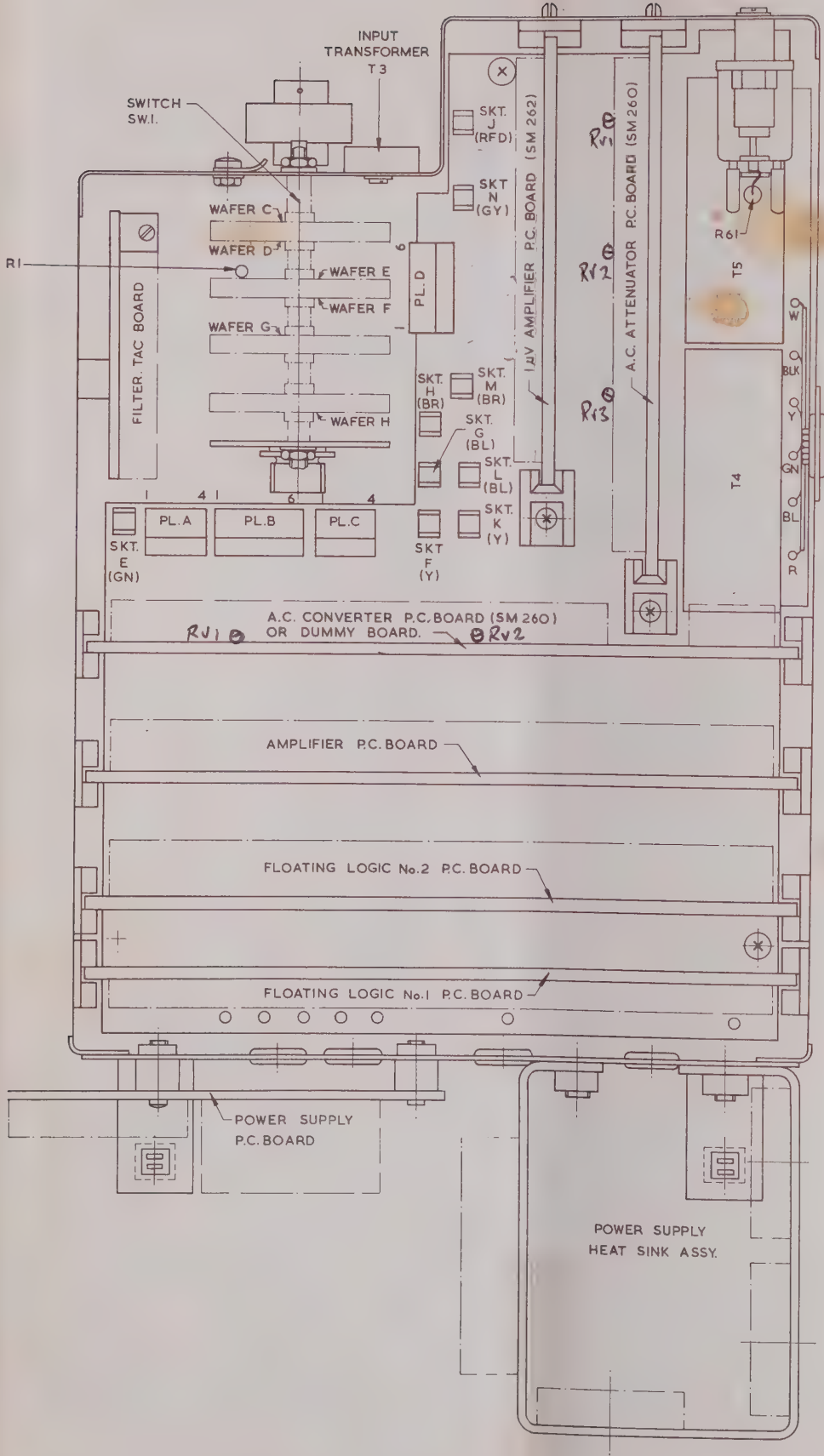
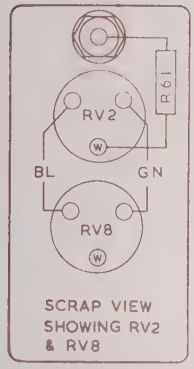


FIG. 1 FLOATING SECTION – CIRCUIT DIAGRAM -E33945

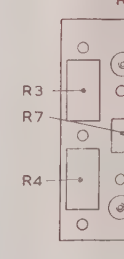




NOTES

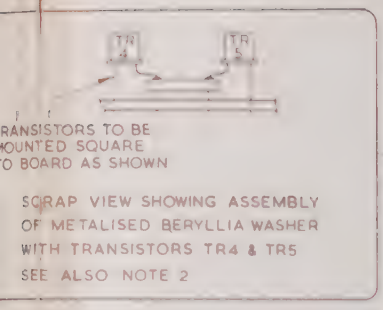
1. FIT TRANSISTOR
TRIO, TR2, TR9, T

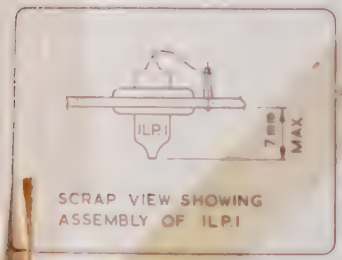
2. TRANSISTORS TR
SOLDERED TO B
ASSEMBLY TO P
TO AVOID DAMA
AND TR5) SPRA
"ARCTN RAY" (
BEFORE OLDER

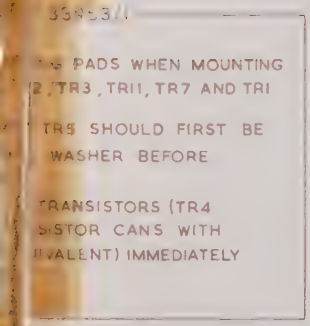


FILTE
COMPONENT

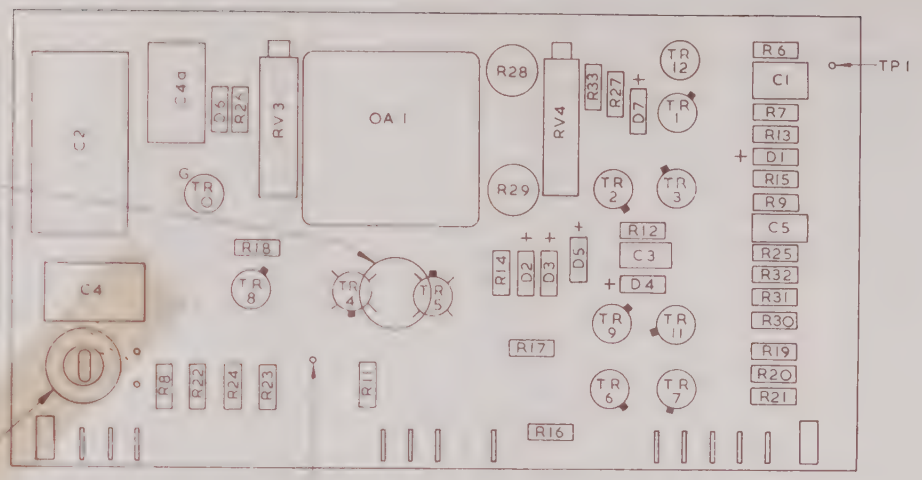
FLOATING BOX - COMPONENT LAYOUT. E33871/1



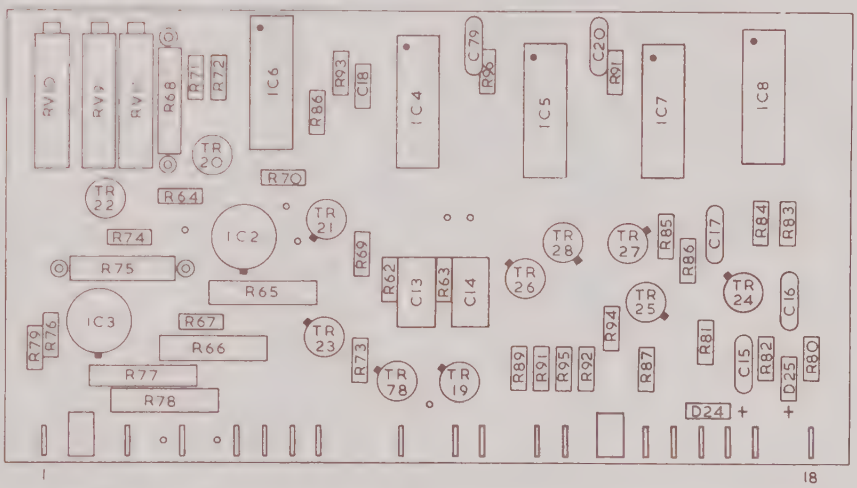




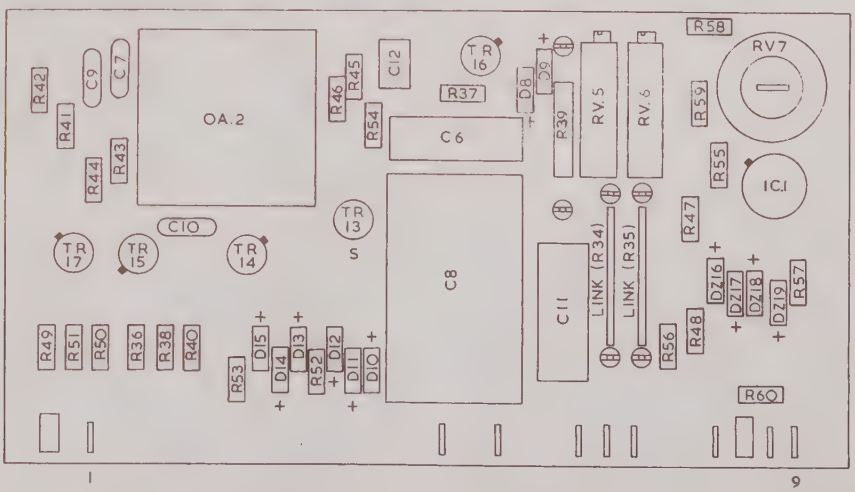
BOARD -
AYOUT C31633/6



INPUT AMPLIFIER BOARD - COMPONENT LAYOUT D33953/1

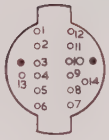


FLOATING LOGIC BOARD No.1 - COMPONENT LAYOUT D33974/1

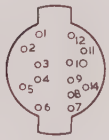


FLOATING LOGIC BOARD No.2 - COMPONENT LAYOUT D33955/1

FIG. 2. FLOATING SECTION - COMPONENT LAYOUTS

FIG. A 

BOTTOM VIEW OF TUBE AS SUPPLIED

FIG. B 

BOTTOM VIEW OF TUBE

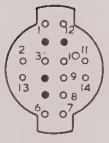
RENEWAL OF INDICATOR TUBES V1 TO V6

(a) REMOVE MOUNTING SPACER.
(b) CUT OFF LEAD MARKED 13 TO WITHIN 1/16" OF BASE OF ENVELOPE (SEE FIG. 'A')
(c) RE-FIT SPACER SO THAT LEADS PASS THROUGH SPACER IN CONFIGURATION SHOWN IN FIG. B ie LEAD 2,5 & 11 ARE RE-POSITIONED.
(d) MOUNT & SOLDER TO P.C. BOARD.

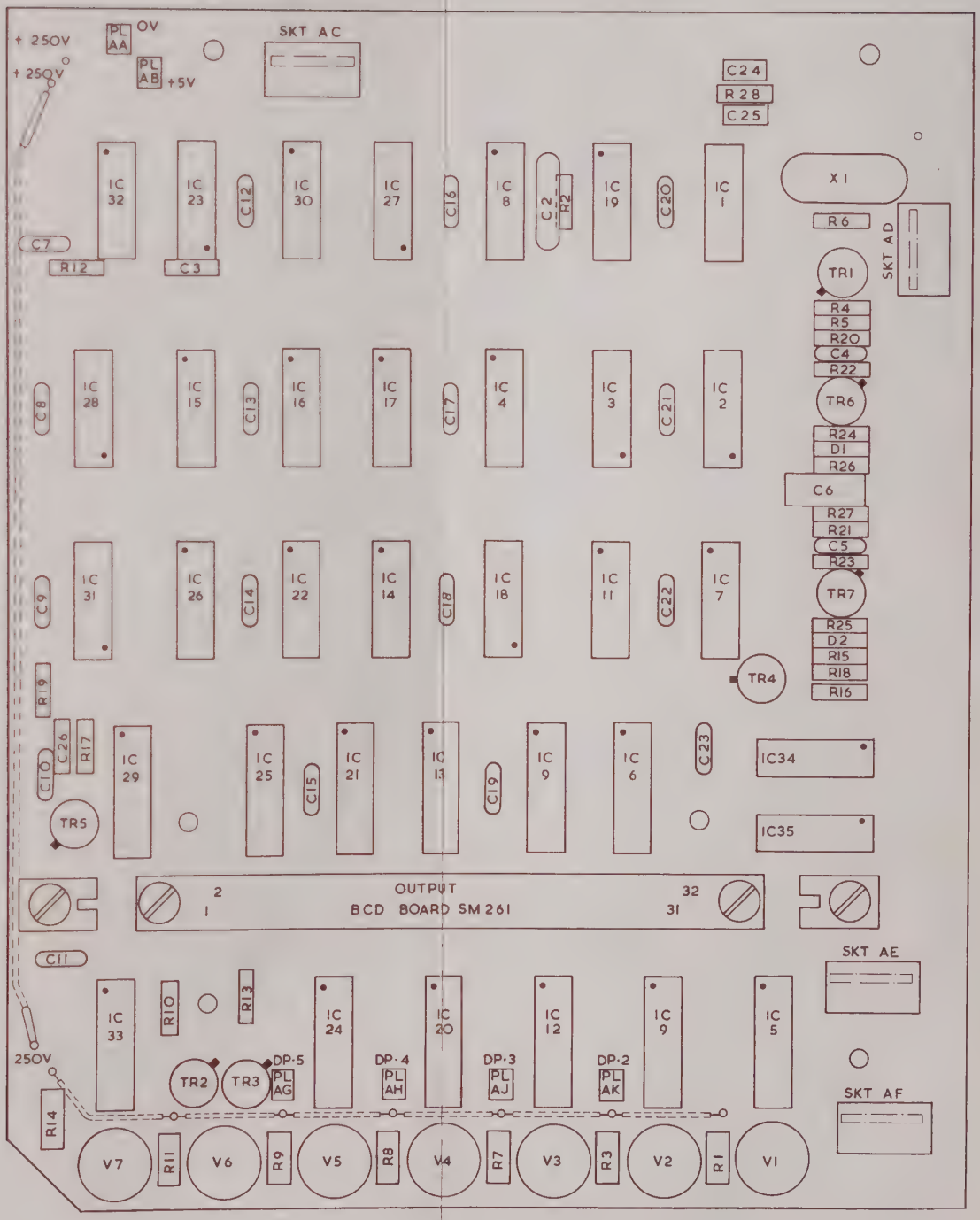
FIG. C

RENEWAL OF INDICATOR TUBE V7

(a) REMOVE MOUNTING SPACER.
(b) RE-FIT SPACER SO THAT LEADS PASS THROUGH SPACER IN CONFIGURATION SHOWN IN FIG 'D'. ie LEADS 2 & 11 RE-POSITIONED.
(c) MOUNT AND SOLDER TO P.C. BOARD.

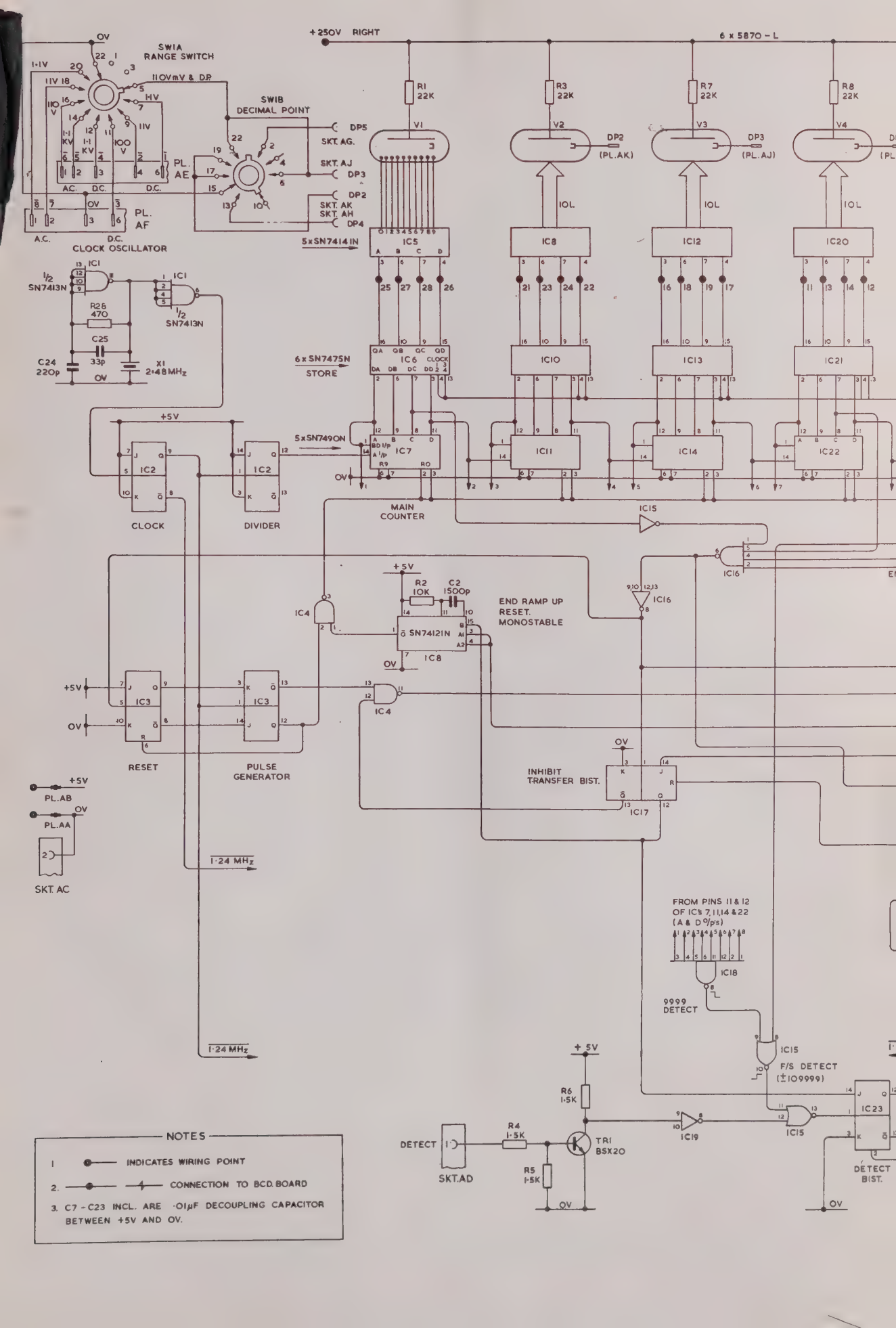
FIG. D 

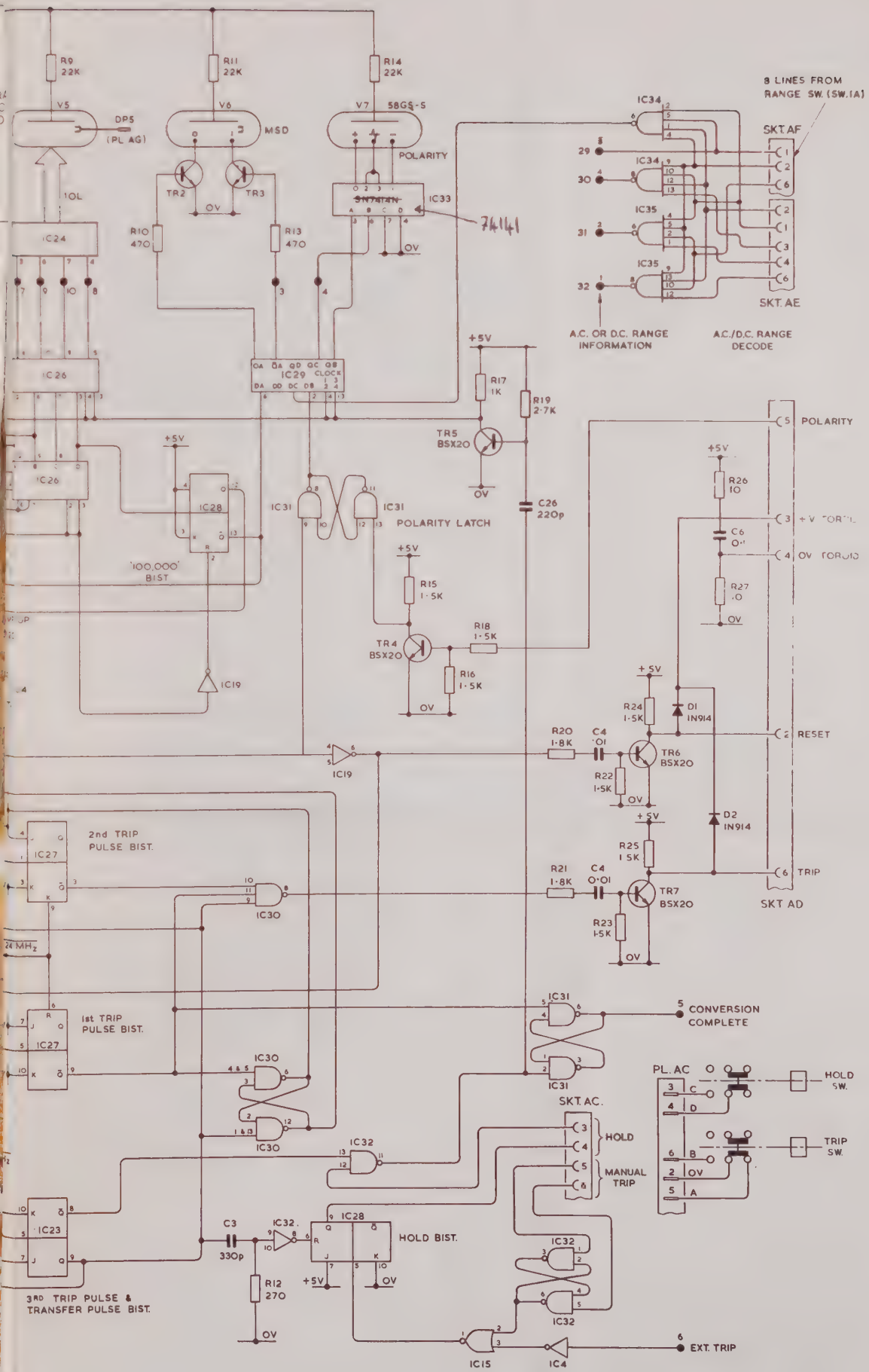
• SYMBOLIZES 'NO PIN'



A.L.I /JAN.74
ISSUE 3

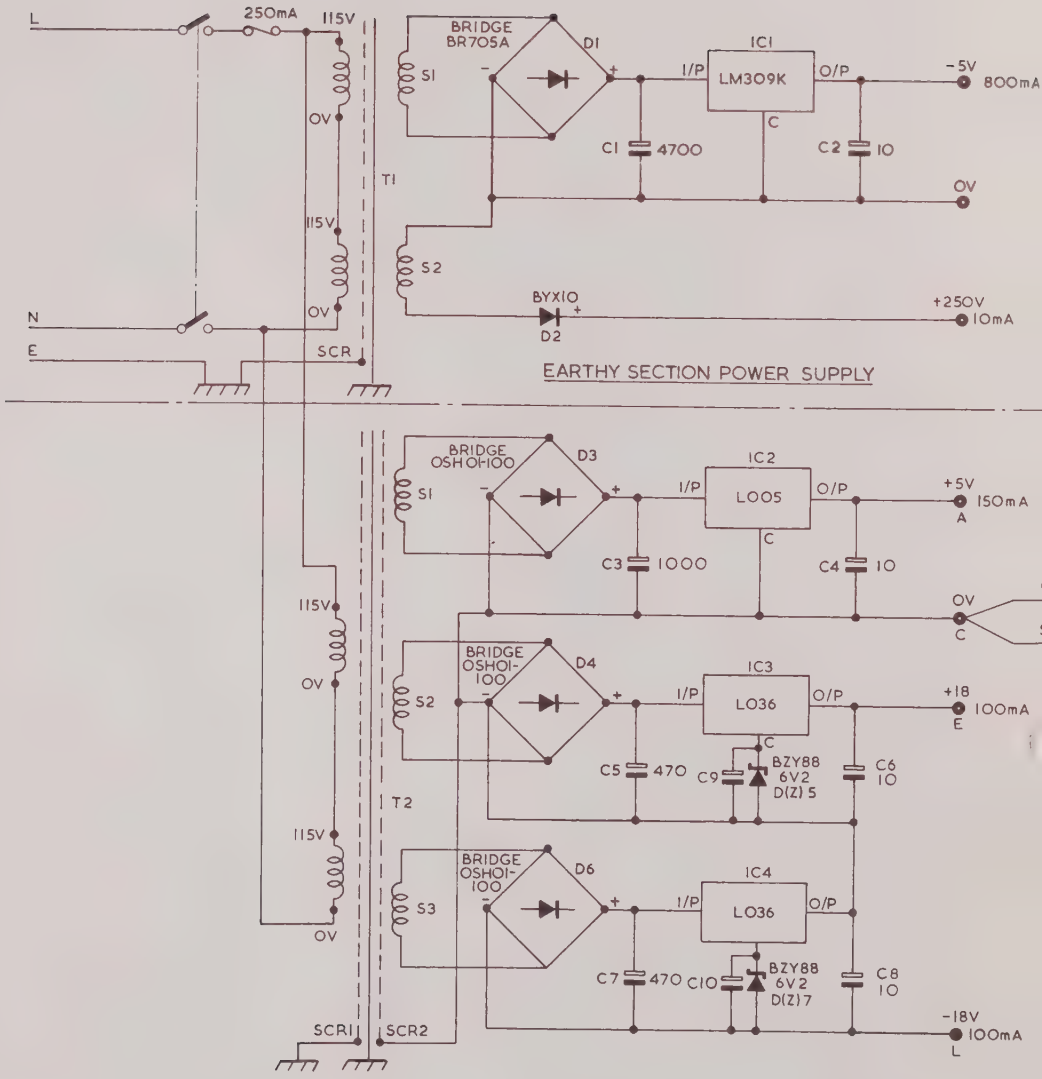
FIG.3 MAIN LOGIC AND DISPLAY BOARD - COMPONENT LAYOUT E.33990


+250V RIGHT
6 x 5870 - L
SW1A RANGE SWITCH
SW1B DECIMAL POINT
CLOCK OSCILLATOR
5 x SN7414 IN
6 x SN7475N STORE
5 x SN7490N
MAIN COUNTER
CLOCK
DIVIDER
RESET
PULSE GENERATOR
END RAMP UP RESET. MONOSTABLE
INHIBIT TRANSFER BIST.
F/S DETECT (±109999)
9999 DETECT
DETECT BIST.
SKT. AC
SKT. AD
1·24 MHz
NOTES
1. INDICATES WIRING POINT
2. CONNECTION TO BCD. BOARD
3. C7 - C23 INCL. ARE ·01μF DECOUPLING CAPACITOR BETWEEN +5V AND OV.



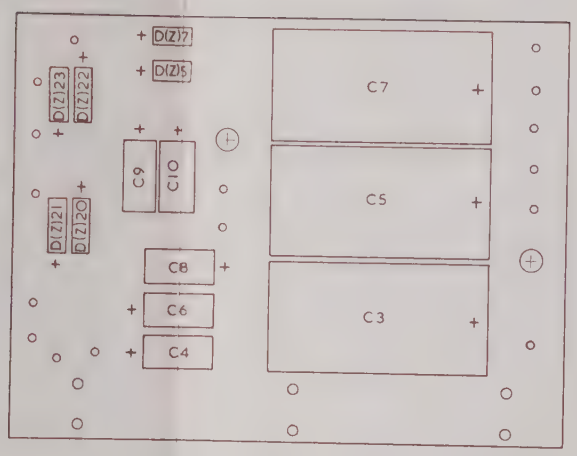
AL1/JAN 74
ISSUE 3

FIG. 4. MAIN LOGIC AND DISPLAY BOARD - CIRCUIT DIAGRAM E40428

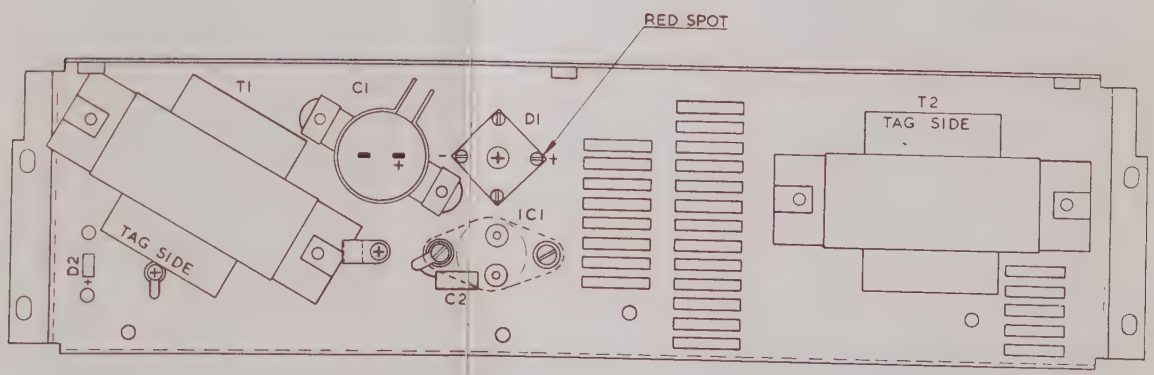


NOTE – IC2, 3 & 4
D3, 4 & 6
MOUNTED ON HEATSINK
ASSY. (SEE P.L. 33886)

CIRCUIT DIAGRAM B.33870/1

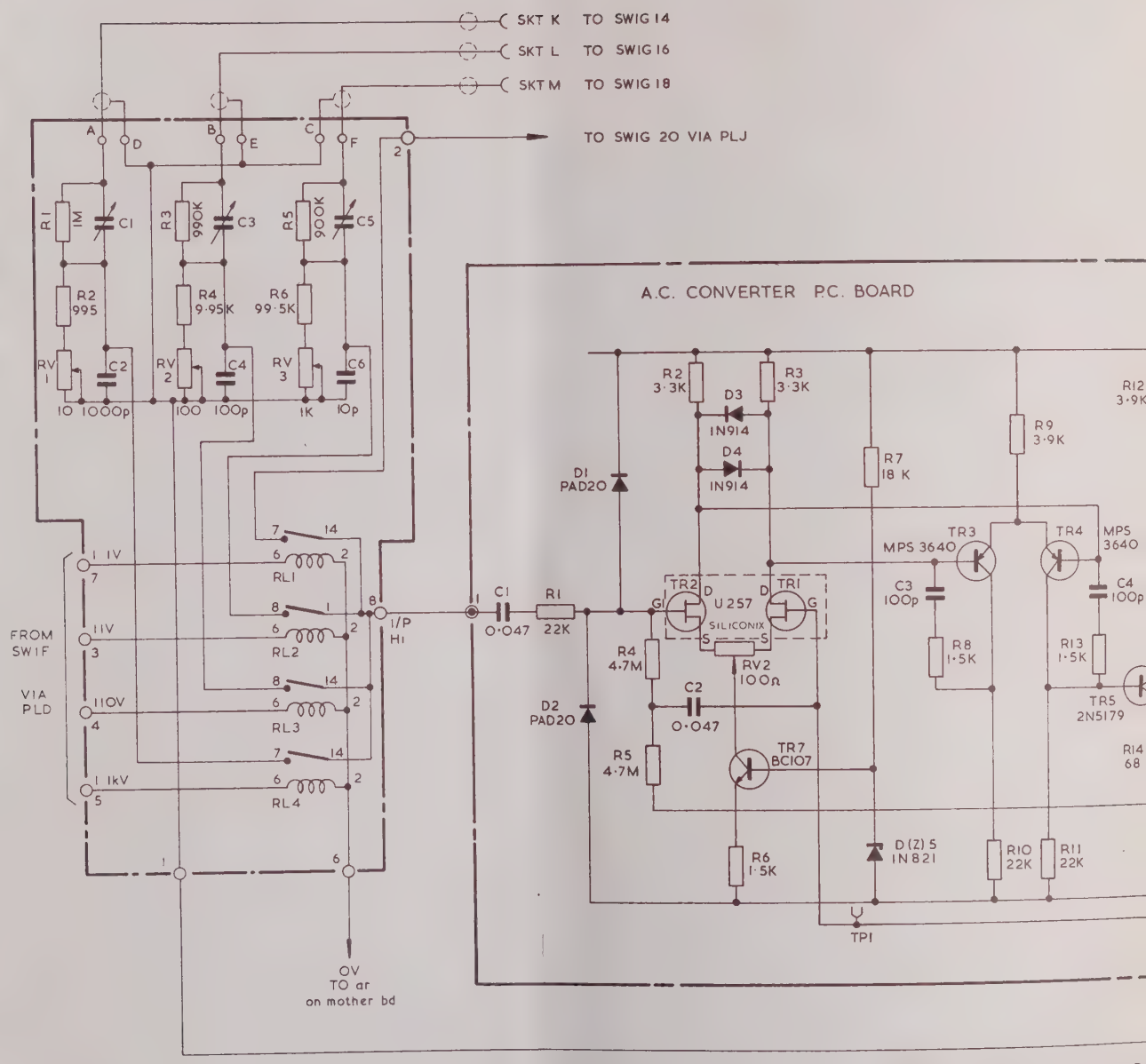


BOARD COMPONENT LAYOUT D33984

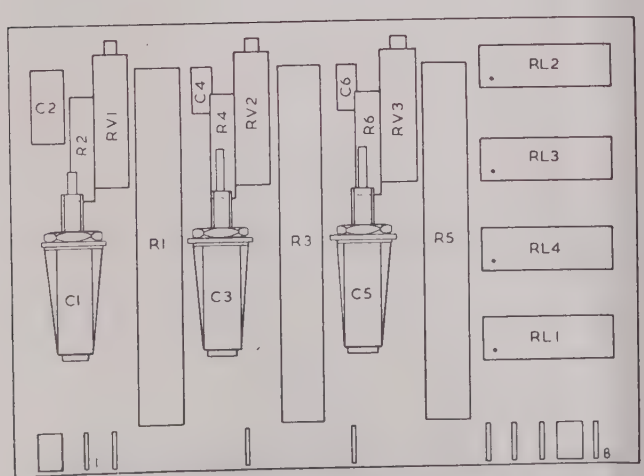


POWER SUPPLY CHASSIS LAYOUT B33888/1

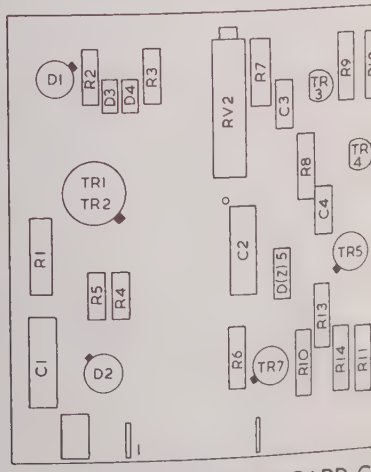
FIG 5 POWER SUPPLY- CIRCUIT AND COMPONENT LAYOUT



CIRCUIT DIAGRAM B3398

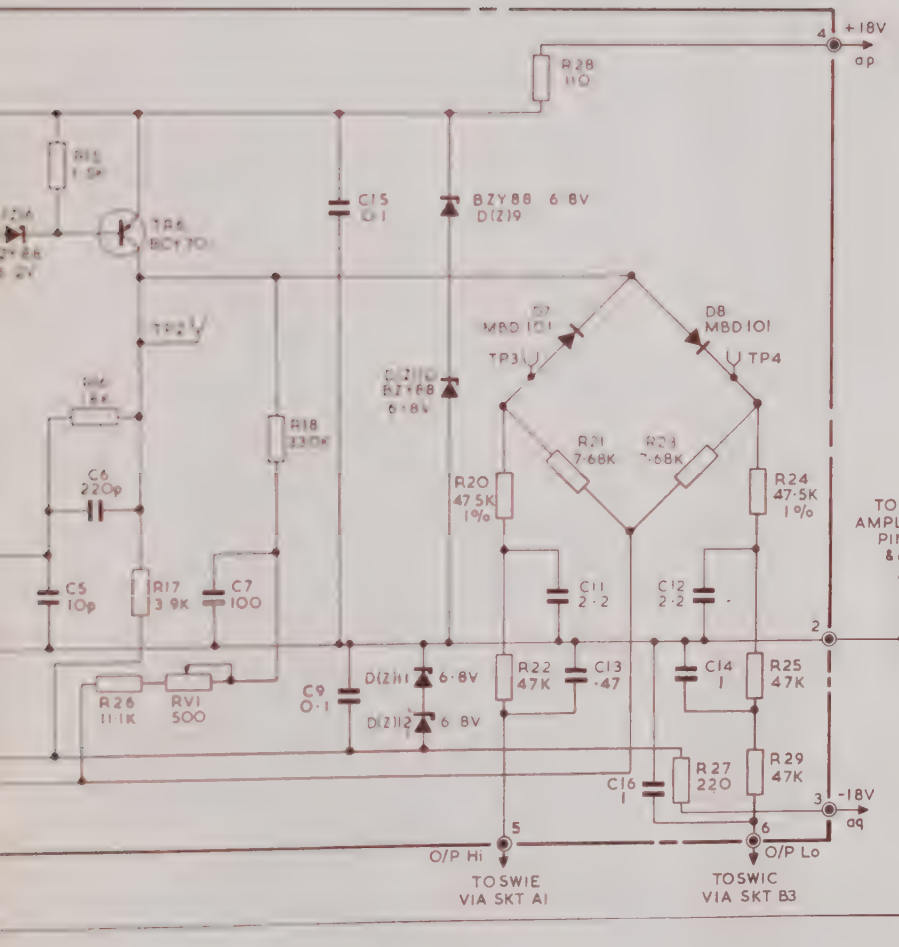


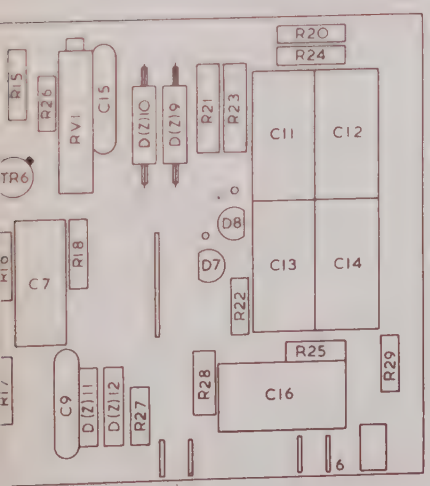
A.C. ATTENUATOR BOARD - COMPONENT LAYOUT D.33978/1



A.C. CONVERTER BOARD-C

FIG. 6 A.C. CONVERTE





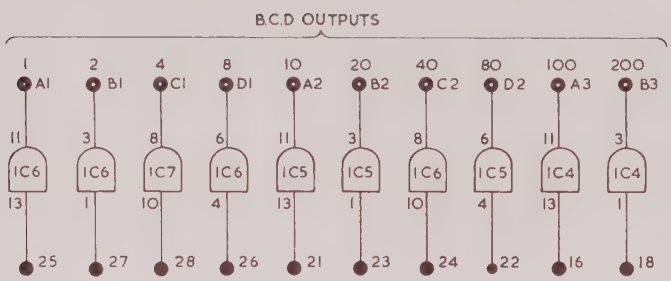
CUT OFF LEAD TO WITHIN
1/32" OF BASE OF ENVELOPE

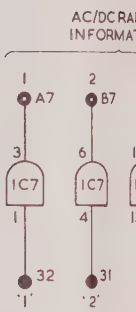
MOD TO TRANSISTOR
TR5 ITEM 67

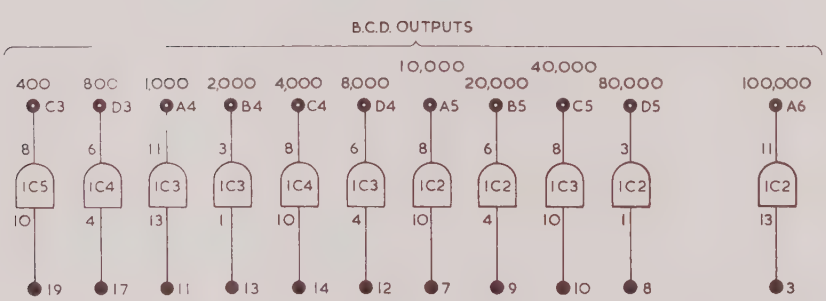
MODIFICATION TO DIODES
D1 & D2 ITEM 88

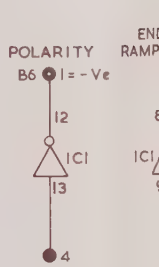
MPONENT LAYOUT D33957/1

(OPTION SM260) – CIRCUIT AND COMPONENT LAYOUT DIAGRAMS

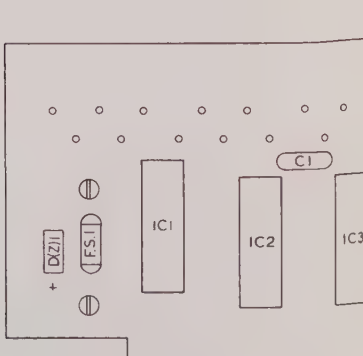






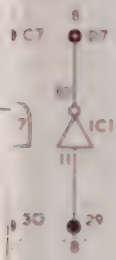


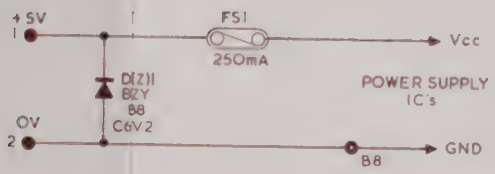
CIRCUIT D

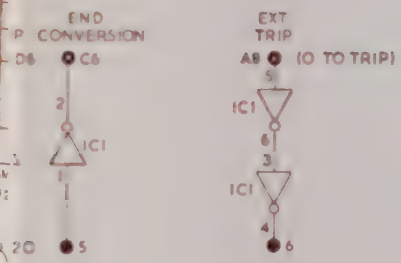


COMPONENT

FIG. 7 B



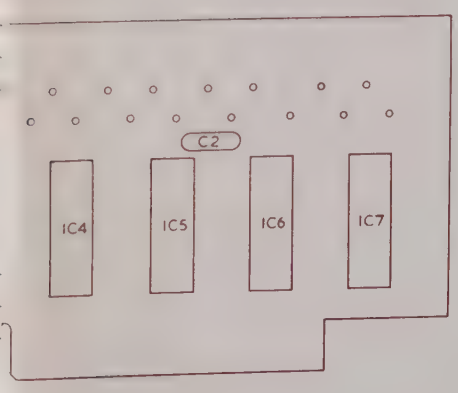




NOTES

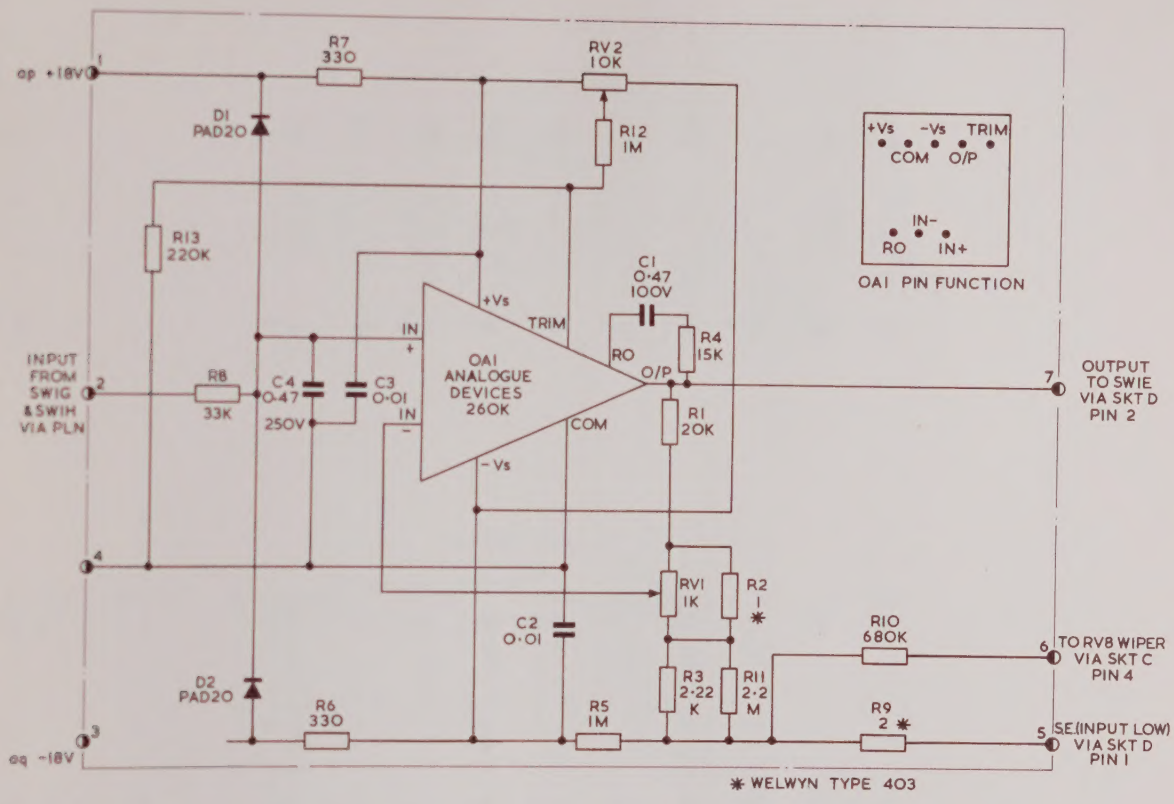
1. INDICATES WIRING POINT (TO B.C.D. SOCKET)
2. P.C.B. EDGE CONTACT.
3. C1 TO C2 INCL. ARE 0·01μF DE - COUPLING CAPACITORS BETWEEN Vcc & GND LINES
4. INVERTERS : SN 7404N AND GATES : SN 7408N

AGRAM B.33986/1

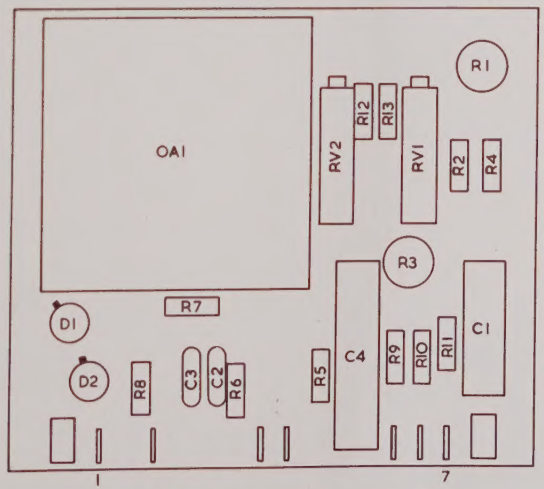


AYOUT D 33951/1

D OUTPUTS UNIT (OPTION SM261)-CIRCUIT & COMPONENT LAYOUT DIAGRAMS



CIRCUIT DIAGRAM D33987/1



COMPONENT LAYOUT D33972

FIG. 8. 1 μV. AMPLIFIER BOARD (OPTION SM262)
- CIRCUIT AND COMPONENT LAYOUT DIAGRAMS

MP MASTER
MA24013

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